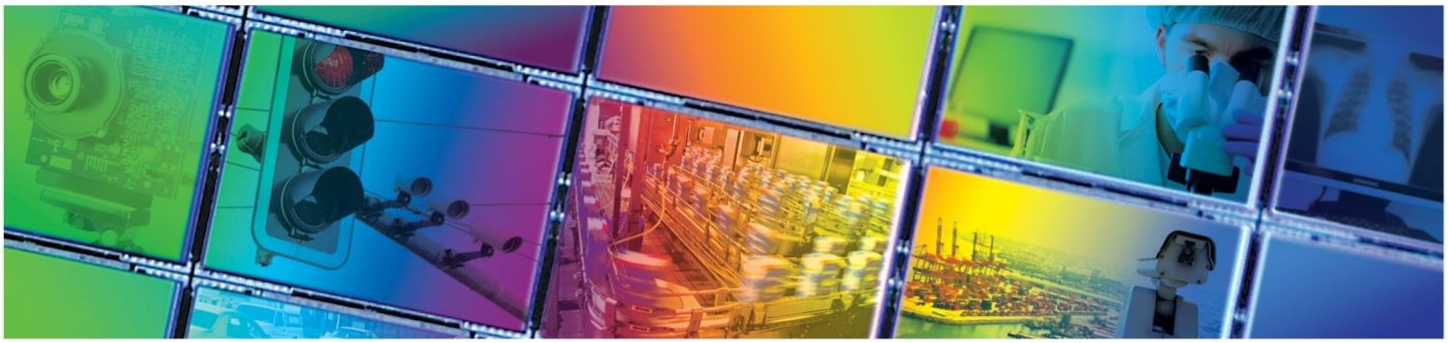
ON Semiconductor®

KAI-04070 IMAGE SENSOR

2048(H) X 2048 (V) INTERLINE CCD IMAGE SENSOR



JUNE 12, 2014

DEVICE PERFORMANCE SPECIFICATION

REVISION 2.1 PS-0145

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KAI-04070 Image Sensor

DESCRIPTION

The KAI-04070 Image Sensor is a 4-megapixel CCD in a 4/3 inch optical format. Based on the TRUESENSE 7.4 micron Interline Transfer CCD Platform, the sensor provides very high smear rejection and up to 82 dB linear dynamic range through the use of a unique dual-gain amplifier. A flexible readout architecture enables use of 1, 2, or 4 outputs for full resolution readout up to 28 frames per second, while a vertical overflow drain structure suppresses image blooming and enables electronic shuttering for precise exposure control.

The sensor is available with the TRUESENSE Sparse Color Filter Pattern, a technology which provides a 2x improvement in light sensitivity compared to a standard color Bayer part.

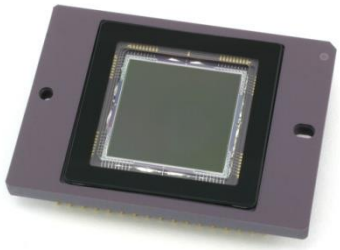
The sensor shares common pin-out and electrical configurations with a full family of Truesense Imaging Interline Transfer CCD image sensors, allowing a single camera design to be leveraged in support of multiple devices.

FEATURES

- Superior smear rejection
- Up to 82 dB linear dynamic range
- Bayer Color Pattern, TRUESENSE Sparse Color Filter Pattern, and Monochrome configurations
- Progressive scan & flexible readout architecture
- High frame rate
- High sensitivity - Low noise architecture
- Package pin reserved for device identification

APPLICATIONS

- Industrial Imaging and Inspection
- Traffic
- Surveillance



Parameter	Typical Value
Architecture	Interline CCD; Progressive Scan
Total Number of Pixels	2128 (H) x 2112 (V)
Number of Effective Pixels	2080 (H) x 2080 (V)
Number of Active Pixels	2048 (H) x 2048 (V)
Pixel Size	7.4 µm (H) x 7.4 µm (V)
Active Image Size	15.2 mm (H) x 15.2 mm (V) 21.4 mm (diag) 4/3 inch format
Aspect Ratio	1:1
Number of Outputs	1, 2, or 4
Charge Capacity	44,000 electrons
Output Sensitivity	8.7 µV/e^- (low), 33 µV/e^- (high)
Quantum Efficiency R, G, B (-CXA, -PXA) Pan (-AXA, -PXA)	 38%, 42%, 43% 52%
Read Noise (f= 40MHz)	12 electrons rms
Dark Current Photodiode VCCD	 3 electrons/s 145 electrons/s
Dark Current Doubling Temp Photodiode VCCD	 7 °C 9 °C
Dynamic Range High gain amp (40 MHz) Dual amp, 2x2 bin (40MHz)	 70 dB 82 dB
Charge Transfer Efficiency	0.999999
Blooming Suppression	> 1000 X
Smear	-115 dB
Image Lag	< 10 electrons
Maximum Pixel Clock Speed	40 MHz
Maximum Frame Rates Quad Output Dual Output Single Output	 28 fps 14 fps 8 fps
Package	68 pin PGA
Cover Glass	AR Coated, 2 Sides

All parameters are specified at T = 40°C unless otherwise noted.

Ordering Information

KAI-04070 Image Sensor

Catalog Number	Product Name	Description	Marking Code
4H2235	KAI-04070-ABA-JD-BA	Monochrome, Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Standard Grade	KAI-04070-ABA Serial Number
4H2236	KAI-04070-ABA-JD-AE	Monochrome, Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Engineering Grade	
4H2339	KAI-04070-ABA-JR-BA	Monochrome, Telecentric Microlens, PGA Package, Taped Clear Cover Glass with AR coating (both sides), Standard Grade	
4H2340	KAI-04070-ABA-JR-AE	Monochrome, Telecentric Microlens, PGA Package, Taped Clear Cover Glass with AR coating (both sides), Engineering Grade	
4H2238	KAI-04070-CBA-JD-BA	Color (Bayer RGB), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Standard Grade	KAI-04070-CBA Serial Number
4H2239	KAI-04070-CBA-JD-AE	Color (Bayer RGB), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Engineering Grade	
4H2241	KAI-04070-PBA-JD-BA	Color (TRUESENSE Sparse CFA), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Standard Grade	KAI-04070-PBA Serial Number
4H2242	KAI-04070-PBA-JD-AE	Color (TRUESENSE Sparse CFA), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Engineering Grade	

Evaluation Support

Catalog Number	Product Name	Description
4H2207	KEM-4H2207-G2 FPGA Board-14-40	FPGA Board for IT-CCD Evaluation Hardware
4H2208	KEH-4H2208-KAI-68 Pin Imager Board	68 Pin Imager Board for IT-CCD Evaluation Hardware
4H2211	KEL-4H2211-Lens Mount Kit	Lens Mount Kit for IT-CCD Evaluation Hardware
4H2269	KEH-4H2269-KAI-68 Pin Narrow Probe Card	68 Pin Probe Card (narrow socket)
4H2268	KEH-4H2268-KAI-68 Pin Wide Probe Card	68 Pin Probe Card (wide socket)

See Application Note *Product Naming Convention* for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.truesenseimaging.com.

Please address all inquiries and purchase orders to:

Truesense Imaging, Inc.
1964 Lake Avenue
Rochester, New York 14615

Phone: (585) 784-5500
E-mail: info@truesenseimaging.com

Device Description

Architecture

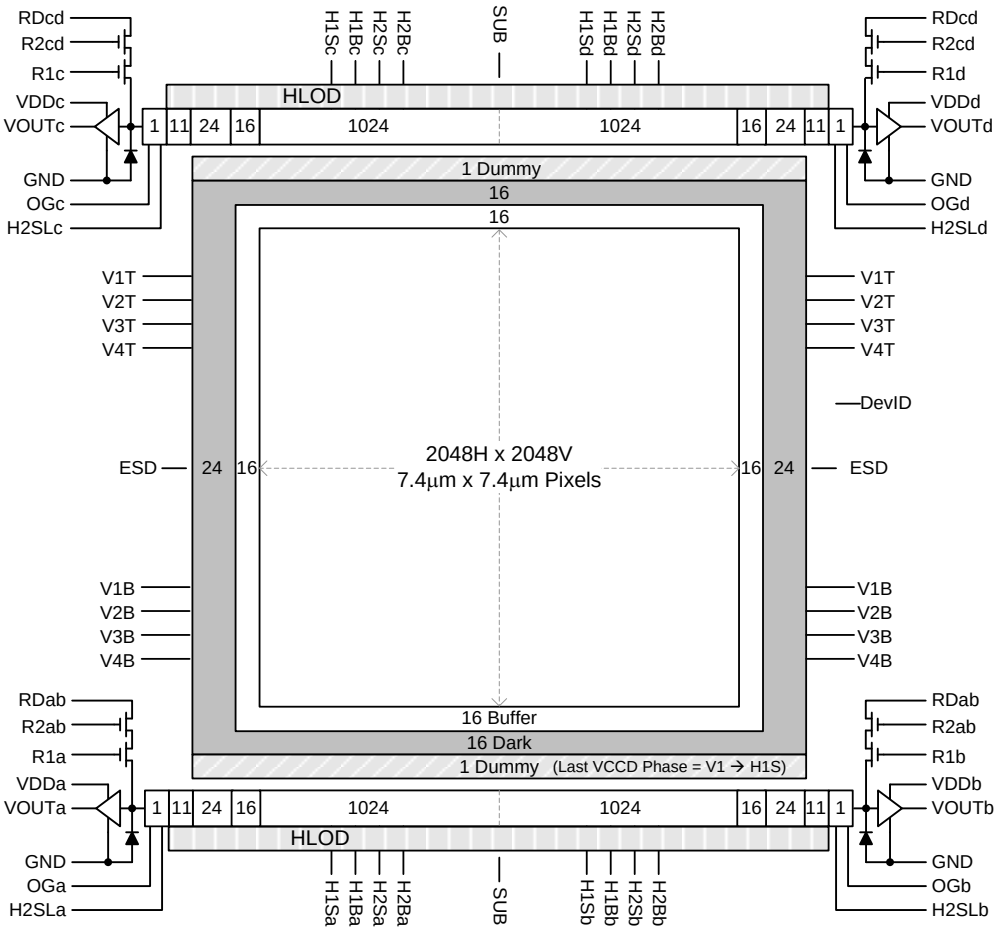


Figure 1: Block Diagram

Dark Reference Pixels

There are 16 dark reference rows at the top and 16 dark rows at the bottom of the image sensor. The 24 dark columns on the left or right side of the image sensor should be used as a dark reference.

Under normal circumstances use only the center 22 columns of the 24 column dark reference due to potential light leakage.

Dummy Pixels

Within each horizontal shift register there are 12 leading additional shift phases. These pixels are designated as dummy pixels and should not be used to determine a dark reference level.

In addition, there is one dummy row of pixels at the top and bottom of the image.

Active Buffer Pixels

16 unshielded pixels adjacent to any leading or trailing dark reference regions are classified as active buffer pixels. These pixels are light sensitive but are not tested for defects and non-uniformities.

Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the individual silicon photodiodes. These photoelectrons are collected locally by the formation of potential wells at each photosite. Below photodiode saturation, the number of photoelectrons collected at each pixel is linearly dependent upon light level and exposure time and non-linearly dependent on wavelength. When the photodiodes charge capacity is reached, excess electrons are discharged into the substrate to prevent blooming

ESD Protection

Adherence to the power-up and power-down sequence is critical. Failure to follow the proper power-up and power-down sequences may cause damage to the sensor. See Power-Up and Power-Down Sequence section.

BAYER COLOR FILTER PATTERN

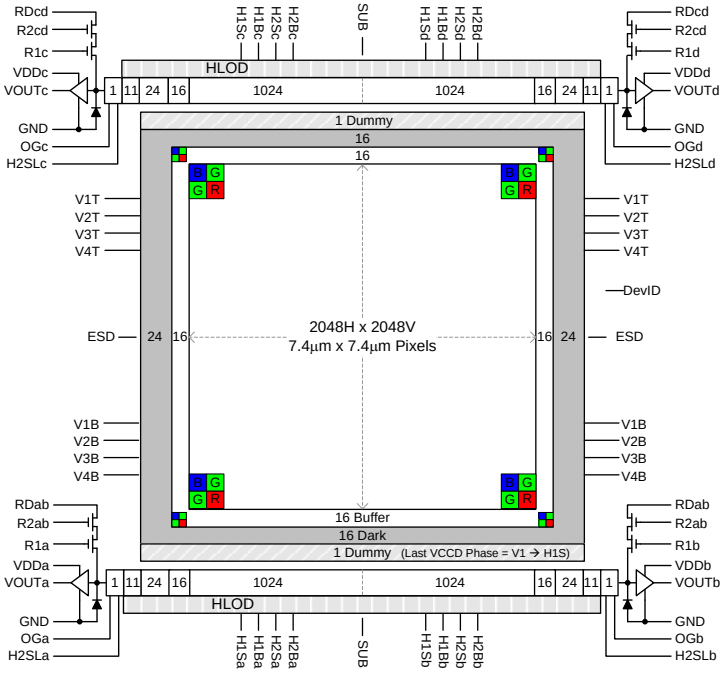


Figure 2: Bayer Color Filter Pattern

TRUESENSE SPARSE COLOR FILTER PATTERN

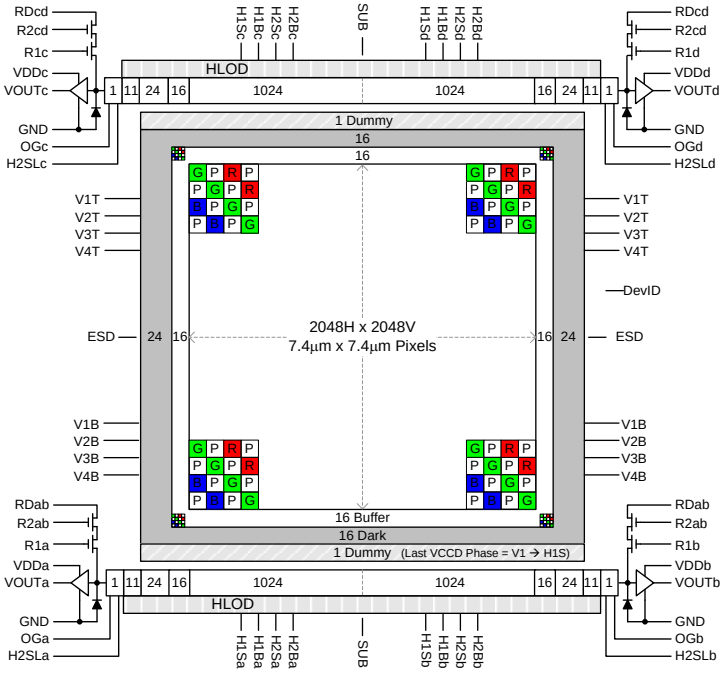


Figure 3: Sparse Color Filter Pattern

PHYSICAL DESCRIPTION

Pin Description and Device Orientation

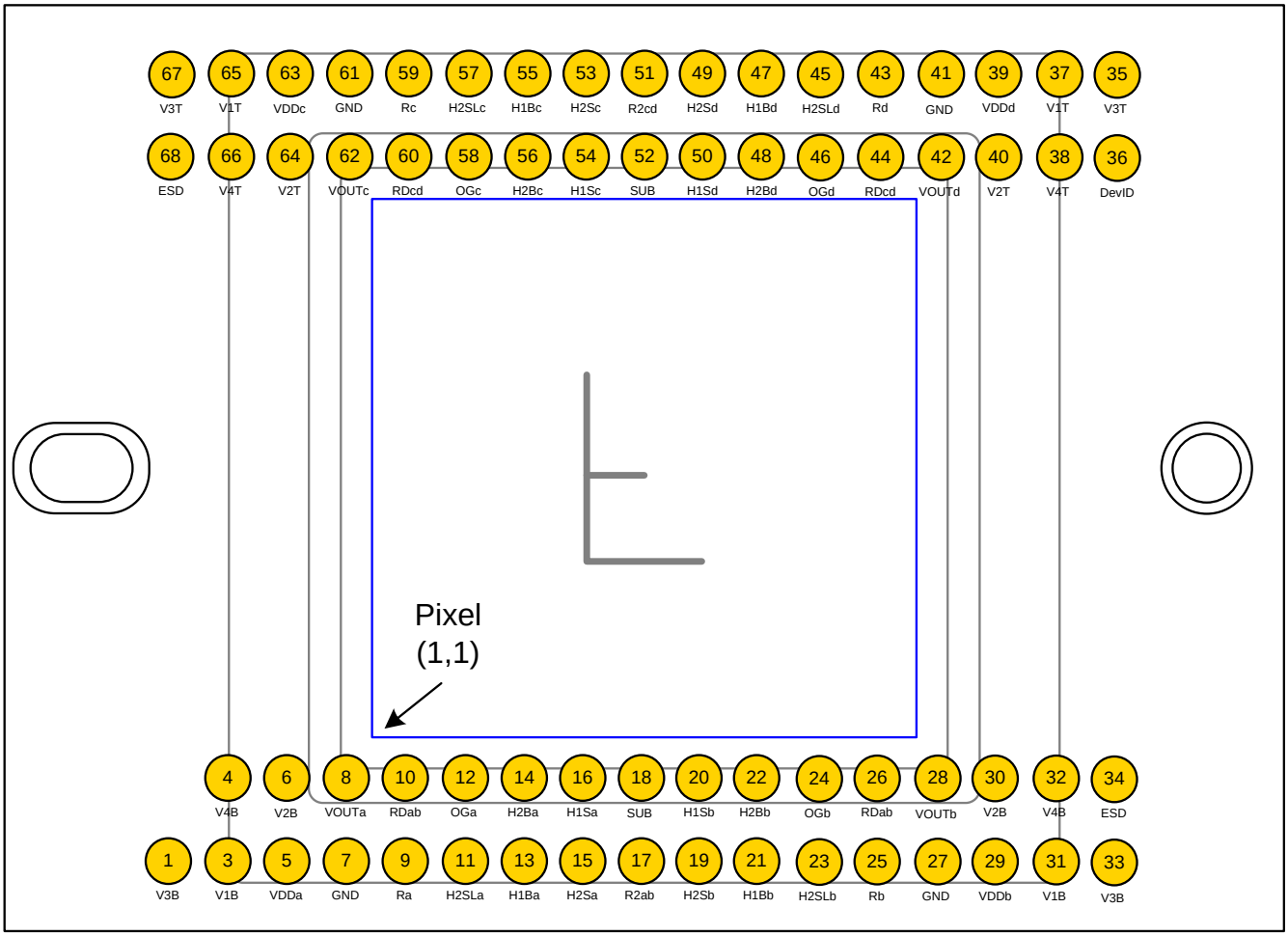


Figure 4: Package Pin Designations - Top View

Pin	Name	Description
1	V3B	Vertical CCD Clock, Phase 3, Bottom
3	V1B	Vertical CCD Clock, Phase 1, Bottom
4	V4B	Vertical CCD Clock, Phase 4, Bottom
5	VDDa	Output Amplifier Supply, Quadrant a
6	V2B	Vertical CCD Clock, Phase 2, Bottom
7	GND	Ground
8	VOUTa	Video Output, Quadrant a
9	Ra	Reset Gate, Standard (high) Gain, Quadrant a
10	RDab	Reset Drain, Quadrants a and b
11	H2SLa	Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant a
12	OGa	Output Gate, Quadrant a
13	H1Ba	Horizontal CCD Clock, Phase 1, Barrier, Quadrant a
14	H2Ba	Horizontal CCD Clock, Phase 2, Barrier, Quadrant a
15	H2Sa	Horizontal CCD Clock, Phase 2, Storage, Quadrant a
16	H1Sa	Horizontal CCD Clock, Phase 1, Storage, Quadrant a
17	R2ab	Reset Gate, Low Gain, Quadrants a and b
18	SUB	Substrate
19	H2Sb	Horizontal CCD Clock, Phase 2, Storage, Quadrant b
20	H1Sb	Horizontal CCD Clock, Phase 1, Storage, Quadrant b
21	H1Bb	Horizontal CCD Clock, Phase 1, Barrier, Quadrant b
22	H2Bb	Horizontal CCD Clock, Phase 2, Barrier, Quadrant b
23	H2SLb	Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant b
24	OGb	Output Gate, Quadrant b
25	Rb	Reset Gate, Standard (high) Gain, Quadrant b
26	RDab	Reset Drain, Quadrants a and b
27	GND	Ground
28	VOUTb	Video Output, Quadrant b
29	VDDb	Output Amplifier Supply, Quadrant b
30	V2B	Vertical CCD Clock, Phase 2, Bottom
31	V1B	Vertical CCD Clock, Phase 1, Bottom
32	V4B	Vertical CCD Clock, Phase 4, Bottom
33	V3B	Vertical CCD Clock, Phase 3, Bottom
34	ESD	ESD Protection Disable

Pin	Name	Description
68	ESD	ESD Protection Disable
67	V3T	Vertical CCD Clock, Phase 3, Top
66	V4T	Vertical CCD Clock, Phase 4, Top
65	V1T	Vertical CCD Clock, Phase 1, Top
64	V2T	Vertical CCD Clock, Phase 2, Top
63	VDDc	Output Amplifier Supply, Quadrant c
62	VOUTc	Video Output, Quadrant c
61	GND	Ground
60	RDcd	Reset Drain, Quadrants c and d
59	Rc	Reset Gate, Standard (high) Gain, Quadrant c
58	OGc	Output Gate, Quadrant c
57	H2SLc	Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant c
56	H2Bc	Horizontal CCD Clock, Phase 2, Barrier, Quadrant c
55	H1Bc	Horizontal CCD Clock, Phase 1, Barrier, Quadrant c
54	H1Sc	Horizontal CCD Clock, Phase 1, Storage, Quadrant c
53	H2Sc	Horizontal CCD Clock, Phase 2, Storage, Quadrant c
52	SUB	Substrate
51	R2cd	Reset Gate, Low Gain, Quadrants c and d
50	H1Sd	Horizontal CCD Clock, Phase 1, Storage, Quadrant d
49	H2Sd	Horizontal CCD Clock, Phase 2, Storage, Quadrant d
48	H2Bd	Horizontal CCD Clock, Phase 2, Barrier, Quadrant d
47	H1Bd	Horizontal CCD Clock, Phase 1, Barrier, Quadrant d
46	OGd	Output Gate, Quadrant b
45	H2SLd	Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant d
44	RDcd	Reset Drain, Quadrants c and d
43	Rd	Reset Gate, Standard (high) Gain, Quadrant d
42	VOUTd	Video Output, Quadrant d
41	GND	Ground
40	V2T	Vertical CCD Clock, Phase 2, Top
39	VDDd	Output Amplifier Supply, Quadrant d
38	V4T	Vertical CCD Clock, Phase 4, Top
37	V1T	Vertical CCD Clock, Phase 1, Top
36	DevID	Device Identification
35	V3T	Vertical CCD Clock, Phase 3, Top

Notes:

1. Liked named pins are internally connected and should have a common drive signal.

Imaging Performance

Typical Operation Conditions

Unless otherwise noted, the Imaging Performance Specifications are measured using the following conditions.

Description	Condition	Notes
Light Source	Continuous red, green and blue LED illumination	1
Operation	Nominal operating voltages and timing	

Notes:
1. For monochrome sensor, only green LED used.

Specifications

All Configurations

Description	Symbol	Min.	Nom.	Max.	Units	Sampling Plan	Temperature Tested At (°C)	Notes
Dark Field Global Non-Uniformity	DSNU	-	-	2.0	mVpp	Die	27, 40	
Bright Field Global Non-Uniformity		-	2.0	5.0	%rms	Die	27, 40	1
Bright Field Global Peak to Peak Non-Uniformity	PRNU	-	5.0	15.0	%pp	Die	27, 40	1
Bright Field Center Non-Uniformity		-	1.0	2.0	%rms	Die	27, 40	1
Maximum Photo-response Nonlinearity High Gain (4,000 to 20,000 electrons) High Gain (4,000 to 40,000 electrons) Low Gain (8,000 to 80,000 electrons)	 NL_HG1 NL_HG2 NL_LG1	 - - -	 2 3 6	 - - -	 % % %	Design		
Maximum Gain Difference Between Outputs	ΔG	-	-	10	%	Design		2
Horizontal CCD Charge Capacity	HNe	-	90	-	ke^-	Design		
Vertical CCD Charge Capacity	VNe	-	60	-	ke^-	Design		
Photodiode Charge Capacity	PNe	-	44	-	ke^-	Die	27, 40	3
Floating Diffusion Capacity – High Gain	FNe_HG	40	-	-	ke^-	Die	27, 40	
Floating Diffusion Capacity – Low Gain	FNe_LG	160	-	-	ke^-	Die	27, 40	
Horizontal CCD Charge Transfer Efficiency	HCTE	0.999995	0.999999	-		Die		
Vertical CCD Charge Transfer Efficiency	VCTE	0.999995	0.999999	-		Die		
Photodiode Dark Current	Ipd	-	7	70	e/p/s	Die	40	
Vertical CCD Dark Current	Ivd	-	140	400	e/p/s	Die	40	
Image Lag	Lag	-	-	10	e^-	Design		
Antiblooming Factor	Xab	1000	-	-		Design		
Vertical Smear	Smr	-	-115	-	dB	Design		
Read Noise	n_{e-T}	-	12 45	-	e^-rms	Design	High gain Low gain	4
Dynamic Range, Standard	DR	-	70.5	-	dB	Design		4, 5
Dynamic Range, extended linear dynamic range mode (XLDR)	XLDR	-	82.5	-	dB	Design		4, 5
Output Amplifier DC Offset	V_{odc}	-	9.0	-	V	Die	27, 40	
Output Amplifier Bandwidth	f_{-3db}	-	250	-	MHz	Die		6
Output Amplifier Impedance	ROUT	-	127	-	Ohms	Die	27, 40	
Output Amplifier Sensitivity High Gain Low Gain	ΔV/ΔN	 - -	 33 8.7	 - -	 μV/e^-	Design		

KAI-04070-ABA and KAI-04070-PBA Configurations

Description	Symbol	Min.	Nom.	Max.	Units	Sampling Plan	Temperature Tested At (°C)	Notes
Peak Quantum Efficiency	QE_{max}	-	52	-	%	Design		
Peak Quantum Efficiency Wavelength	λQE	-	500	-	nm	Design		

KAI-04070-CBA and KAI-04070-PBA Configurations

Description		Symbol	Min.	Nom.	Max.	Units	Sampling Plan	Temperature Tested At (°C)	Notes
Peak Quantum Efficiency	Blue Green Red	QE_{max}	-	43 42 38	-	%	Design		
Peak Quantum Efficiency Wavelength	Blue Green Red	λQE	-	470 540 620	-	nm	Design		

Notes:

1. Per color
2. Value is over the range of 10% to 100% of linear signal level saturation.
3. The operating value of the substrate voltage, VAB, will be marked on the shipping container for each device. The value of VAB is set such that the photodiode charge capacity is 440 mV. This value is determined while operating the device in the low gain mode. VAB value assigned is valid for both modes; high gain or low gain.
4. At 40 MHz.
5. Uses 20LOG(PNe/n_{e-T})
6. Assumes 5pF load

Linear Signal Range

High Gain

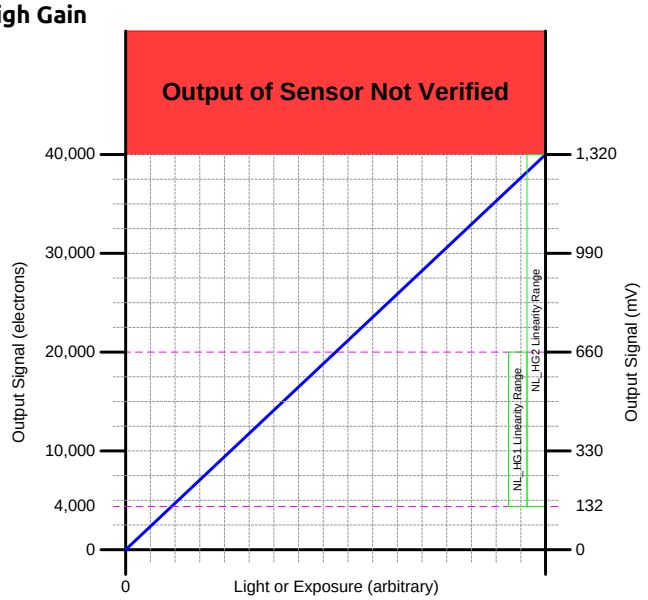


Figure 5: High Gain Linear Signal Range

Low Gain

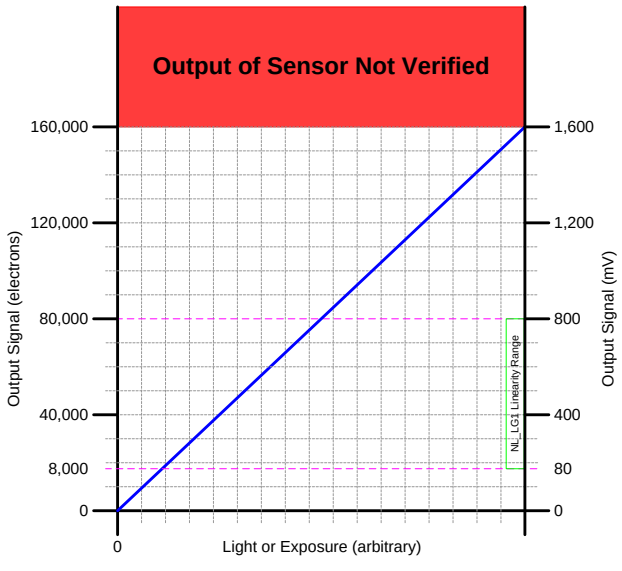


Figure 6: Low Gain Linear Signal Range

Typical Performance Curves

QUANTUM EFFICIENCY

Monochrome with Microlens

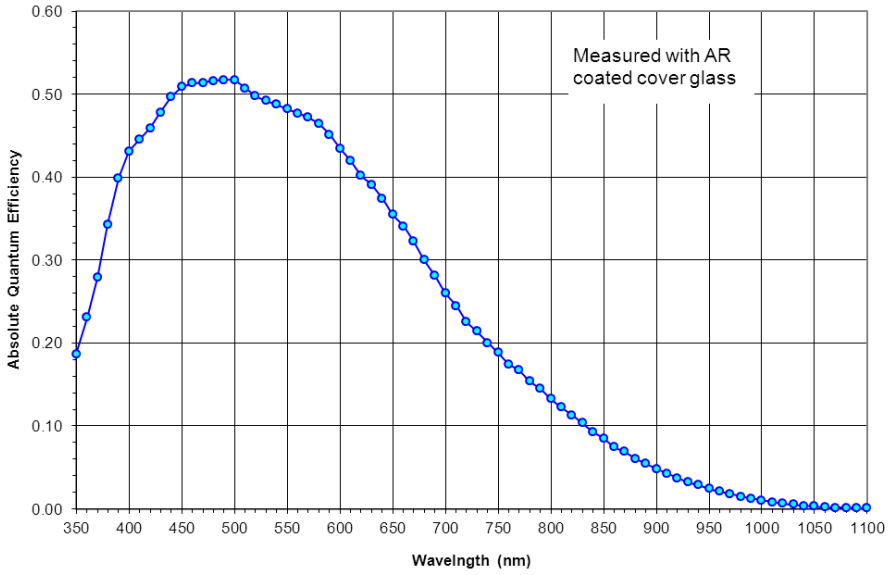


Figure 7: Monochrome with Microlens Quantum Efficiency

Color (Bayer RGB) with Microlens

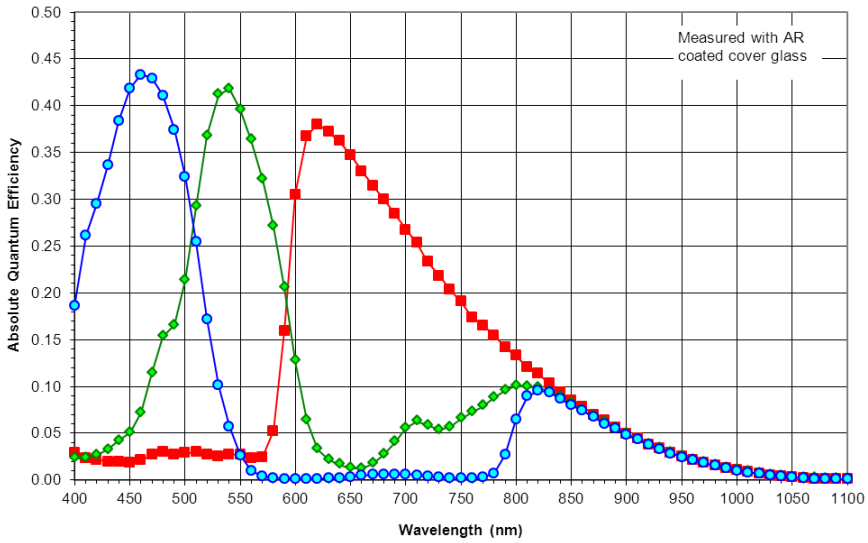


Figure 8: Color (Bayer RGB) with Microlens Quantum Efficiency

Color (TRUESENSE Sparse CFA) with Microlens

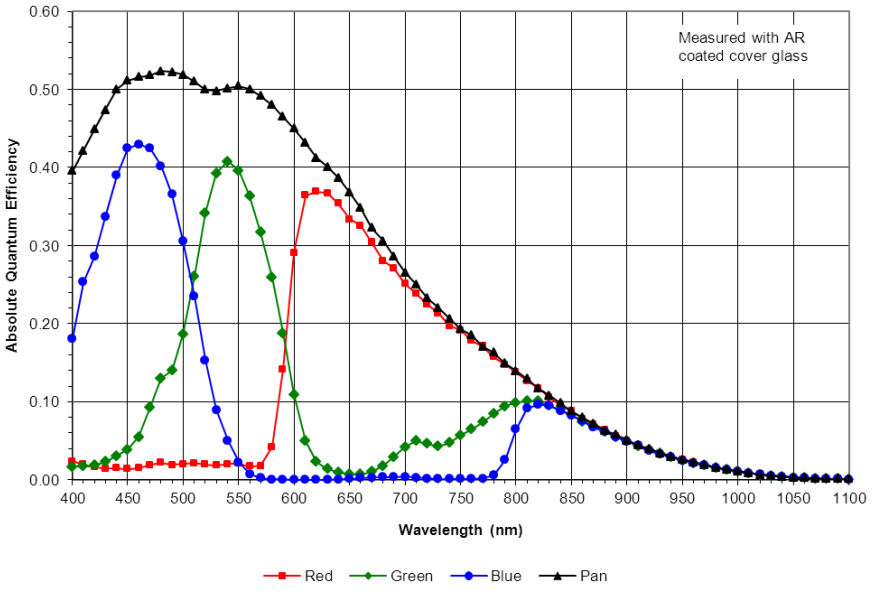


Figure 9: Color (TRUESENSE Sparse CFA) with Microlens Quantum Efficiency

ANGULAR QUANTUM EFFICIENCY

For the curves marked “Horizontal”, the incident light angle is varied in a plane parallel to the HCCD.

For the curves marked “Vertical”, the incident light angle is varied in a plane parallel to the VCCD.

Monochrome with Microlens

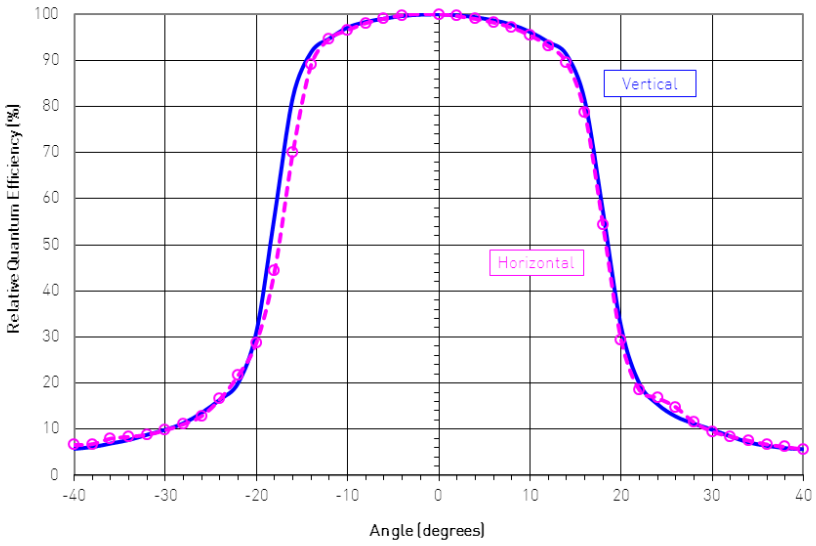


Figure 10: Monochrome with Microlens Angular Quantum Efficiency

Color (Bayer RGB) with Microlens

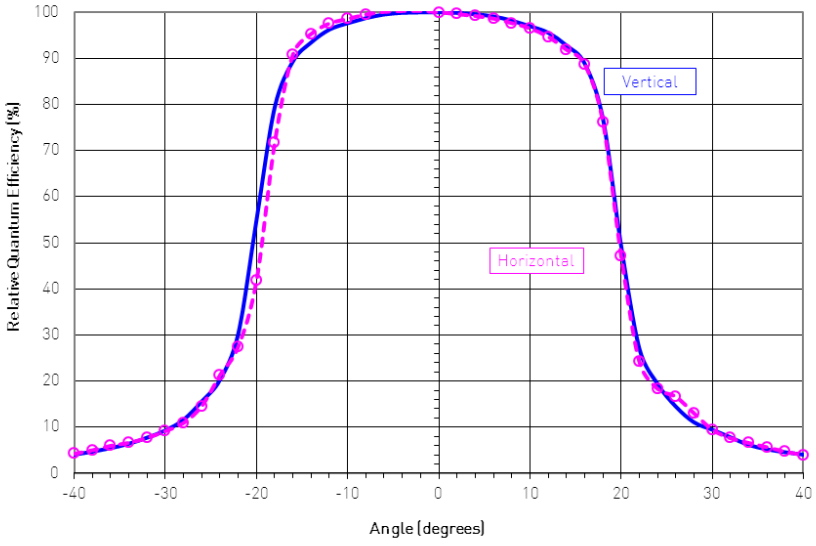


Figure 11: Color (Bayer RGB) with Microlens Angular Quantum Efficiency

DARK CURRENT VERSUS TEMPERATURE

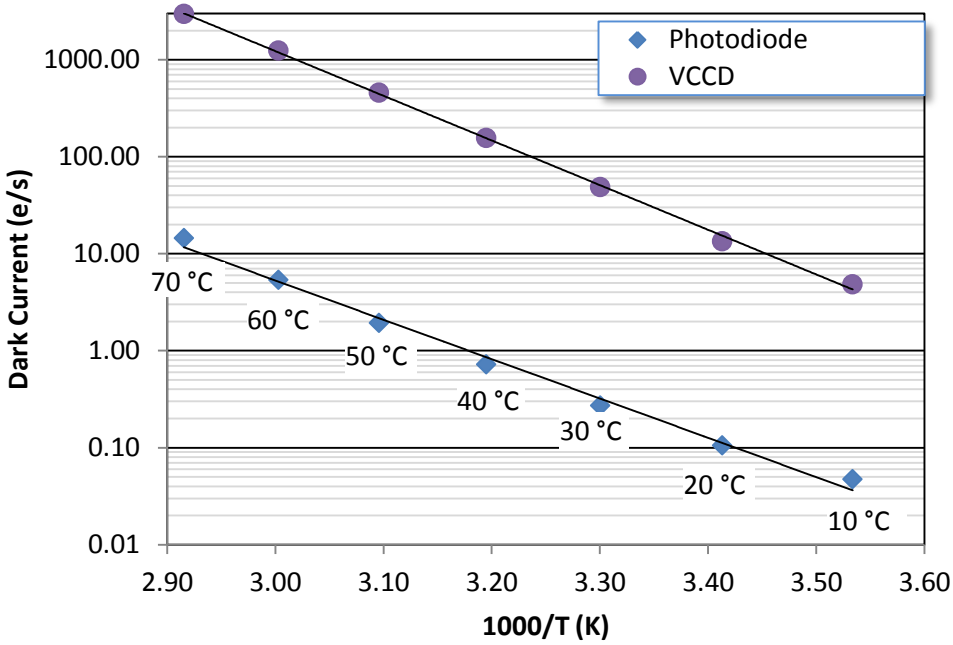


Figure 12: Dark Current versus Temperature

POWER – ESTIMATED

Power – Estimated – Full Resolution

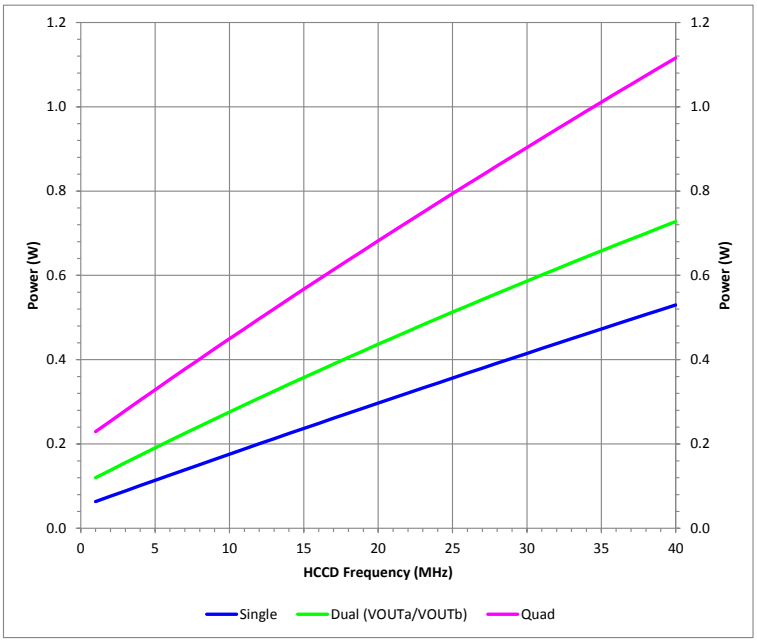


Figure 13: Power – Full Resolution

Power – Estimated – 1/4 Resolution – 2x2 Binning

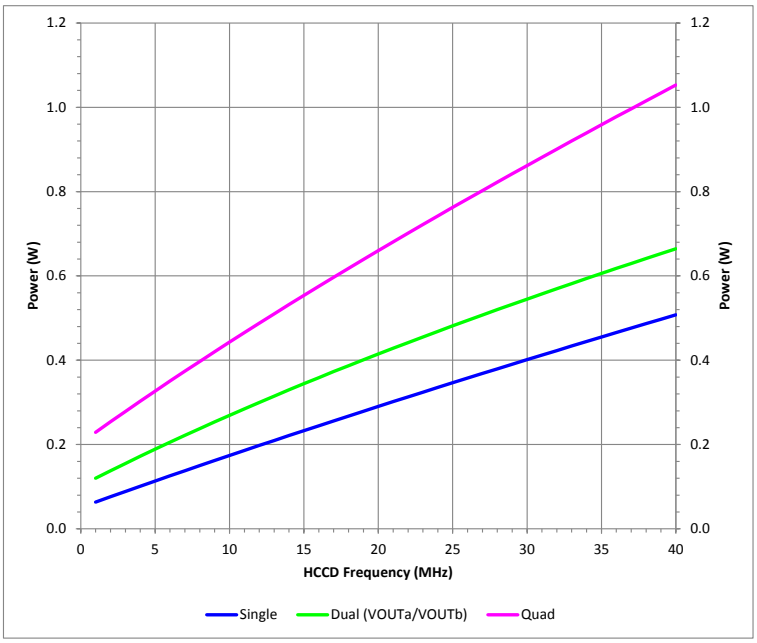


Figure 14: Power – 1/4 Resolution – Constant HCCD

Power – 1/4 Resolution – 2x2 Binning using Variable HCCD XLDR

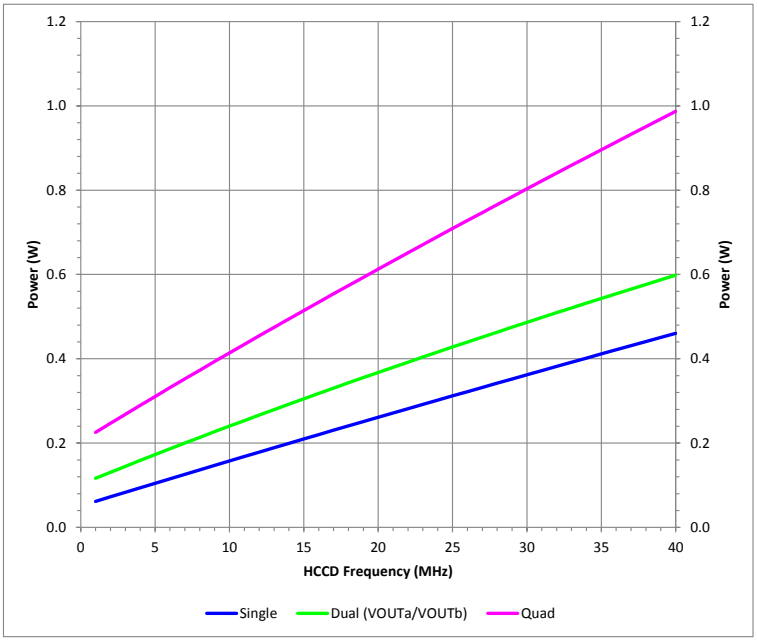


Figure 15: Power – 1/4 Resolution – Variable HCCD XLDR

Power – 1/4 Resolution – 2x2 Binning using Constant XLDR

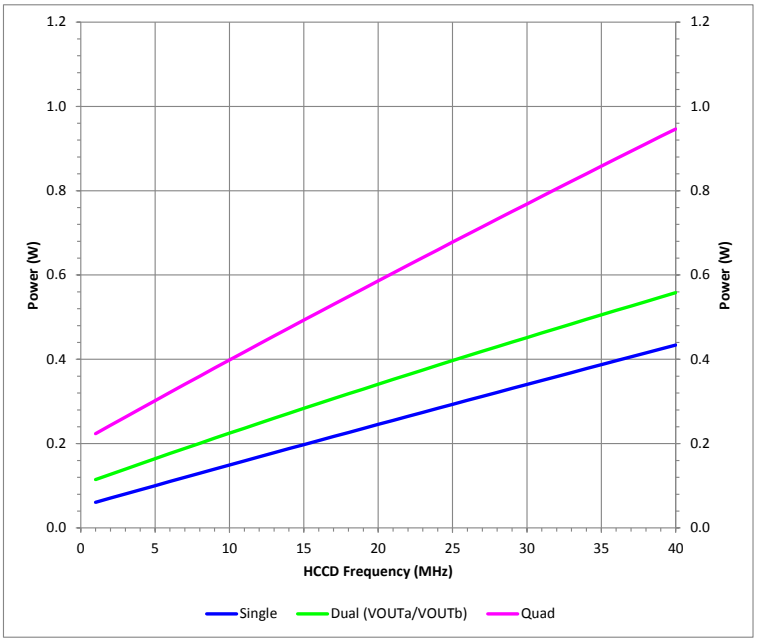


Figure 16: Power – 1/4 Resolution - Constant HCCD XLDR

FRAME RATES

Frame Rates – Full Resolution

Frame rates are for low and high gain modes of operation.

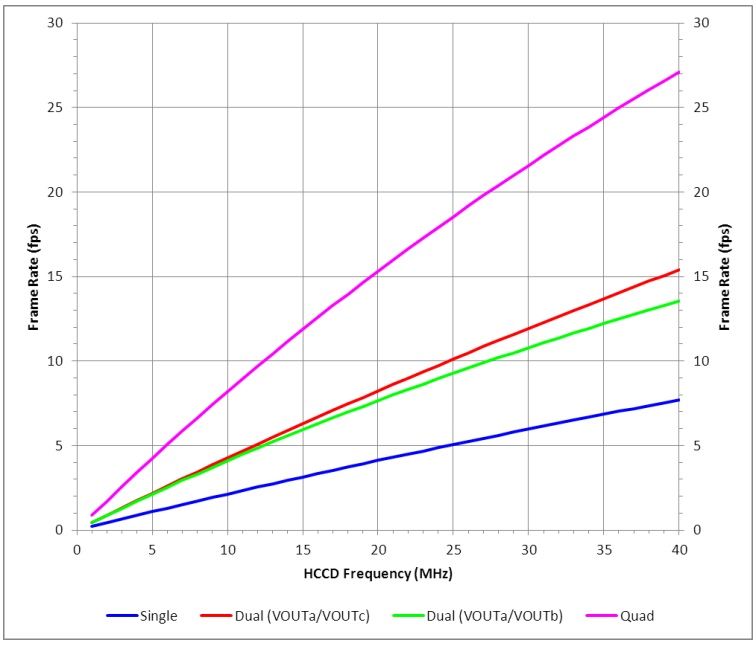


Figure 17: Frame Rates – Full Resolution

Frame Rates – 1/4 Resolution – 2x2 Binning

Frame rates for low gain and high gain modes of operation

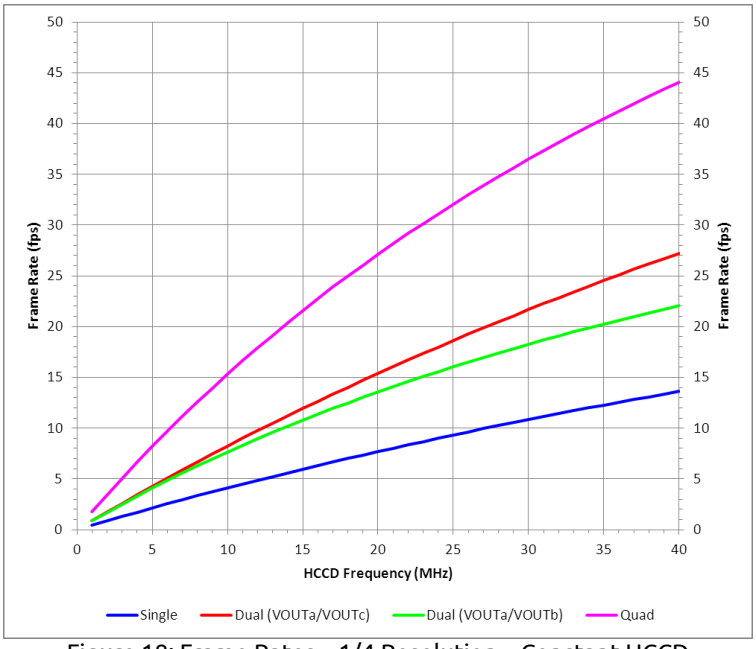


Figure 18: Frame Rates – 1/4 Resolution – Constant HCCD

Frame Rates – 1/4 Resolution – 2x2 Binning using Variable HCCD XLDR

Frame rates for variable HCCD mode of operation

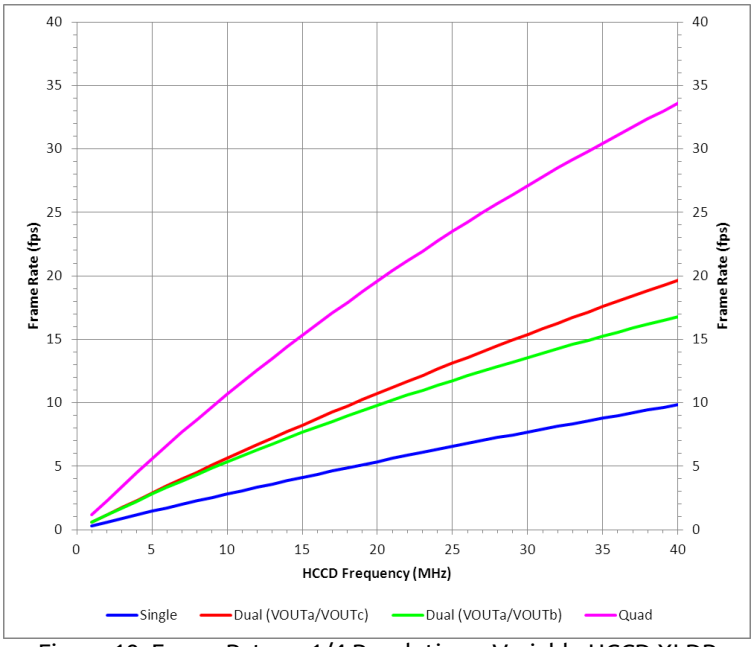


Figure 19: Frame Rates – 1/4 Resolution – Variable HCCD XLDR

Frame Rates – 1/4 Resolution – 2x2 Binning using Constant XLDR

Frame rates for a constant HCCD mode of operation

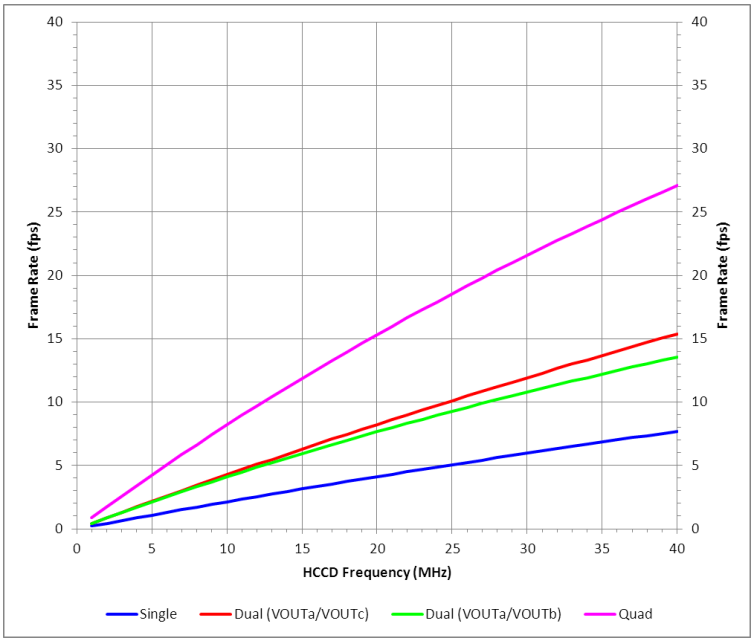


Figure 20: Frame Rates – 1/4 Resolution - Constant HCCD XLDR

Defect Definitions

Operation Conditions for Defect Testing at 40 °C

Description	Condition	Notes
Operational Mode	One output, using VOUTa, continuous readout	
HCCD Clock Frequency	20 MHz	
Pixels Per Line	2140	
Lines Per Frame	2112	
Line Time	115.0µsec	
Frame Time	242.9 msec	
Photodiode Integration Time(PD_Tint)	PD_Tint = Frame Time = 242.9 msec, no electronic shutter used	
Temperature	40°C	
Light Source	Continuous red, green and blue LED illumination	1
Operation	Nominal operating voltages and timing	

Notes
1. For monochrome sensor, only the green LED is used.

Defect Definitions for Testing at 40 °C

Description	Definition	Standard Grade	Notes
Major dark field defective bright pixel	Defect ≥83 mV	40	1
Major bright field defective pixel	-12% ≥ Defect ≥+12%		
Minor dark field defective bright pixel	Defect ≥41 mV	400	
Cluster Defect	A group of 2 to 10 contiguous major defective pixels, but no more than 2 adjacent defects horizontally.	8	2
Column defect	A group of more than 10 contiguous major defective pixels along a single column	0	2

Notes:
1. For the color devices (KAI-04070-CBA and KAI-04070-PBA), a bright field defective pixel deviates by 12% with respect to pixels of the same color.
2. Column and cluster defects are separated by no less than two (2) good pixels in any direction (excluding single pixel defects).

Operation Conditions for Defect Testing at 27 °C

Description	Condition	Notes
Operational Mode	One output, using VOUTa, continuous readout	
HCCD Clock Frequency	20 MHz	
Pixels Per Line	2140	
Lines Per Frame	2112	
Line Time	115µsec	
Frame Time	242.9 msec	
Photodiode Integration Time(PD_Tint)	PD_Tint = Frame Time = 242.9 msec, no electronic shutter used	
Temperature	27°C	
Light Source	Continuous red, green and blue LED illumination	1
Operation	Nominal operating voltages and timing	

Notes
1. For monochrome sensor, only the green LED is used.

Defect Definitions for Testing at 27 °C

Description	Definition	Standard Grade	Notes
Major dark field defective bright pixel	Defect ≥27 mV	40	1
Major bright field defective pixel	-12% ≥ Defect ≥+12%		
Cluster Defect	A group of 2 to 10 contiguous major defective pixels, but no more than 2 adjacent defects horizontally.	8	2
Column defect	A group of more than 10 contiguous major defective pixels along a single column	0	2

Notes:
1. For the color devices (KAI-04070-CBA and KAI-04070-PBA), a bright field defective pixel deviates by 12 % with respect to pixels of the same color.
2. Column and cluster defects are separated by no less than two (2) good pixels in any direction (excluding single pixel defects).

Defect Map

The defect map supplied with each sensor is based upon testing at an ambient (27°C) temperature. Minor point defects are not included in the defect map. All defective pixels are reference to pixel 1, 1 in the defect maps. See Figure 21 for the location of pixel 1, 1.

Test Definitions

Test Regions of Interest

Image Area ROI: Pixel (1, 1) to Pixel (2080, 2080)

Active Area ROI: Pixel (17, 17) to Pixel (2064, 2064)

Center ROI: Pixel (991, 991) to Pixel (1090, 1090)

Only the Active Area ROI pixels are used for performance and defect tests.

OVERCLOCKING

The test system timing is configured such that the sensor is overclocked in both the vertical and horizontal directions. See Figure 21 for a pictorial representation of the regions of interest.

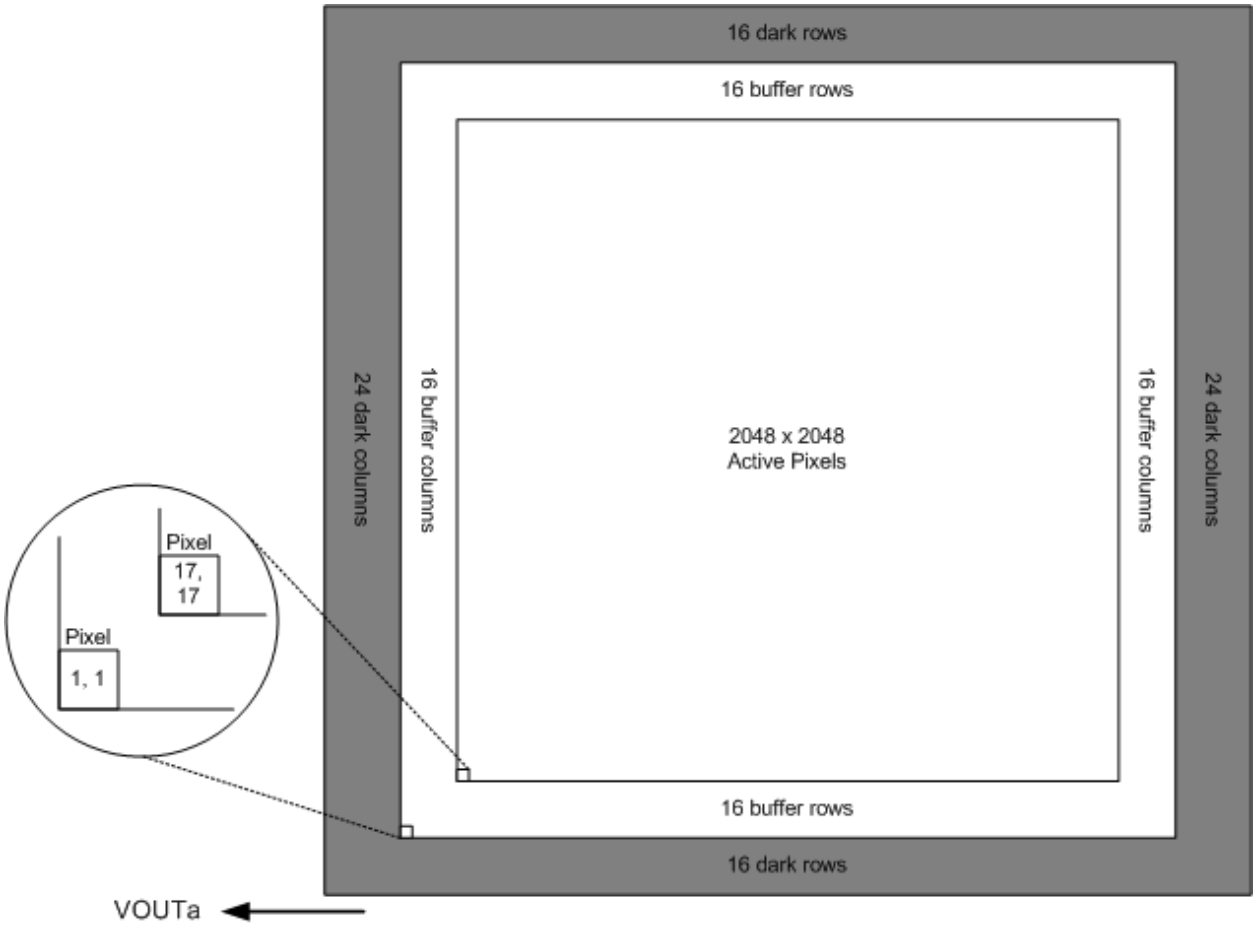


Figure 21: Regions of Interest

TESTS

Dark Field Global Non-Uniformity

This test is performed under dark field conditions. The sensor is partitioned into 256 sub regions of interest, each of which is 128 by 128 pixels in size. The average signal level of each of the 256 sub regions of interest is calculated. The signal level of each of the sub regions of interest is calculated using the following formula:

Signal of ROI[i] = (ROI Average in counts – Horizontal overclock average in counts) * mV per count

where i = 1 to 256. During this calculation on the 256 sub regions of interest, the maximum and minimum signal levels are found. The dark field global uniformity is then calculated as the maximum signal found minus the minimum signal level found.

Units: mVpp (millivolts peak to peak)

Global Non-Uniformity

This test is performed with the imager illuminated to a level such that the output is at 70% of saturation (approximately 924 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 1320 mV. Global non-uniformity is defined as

$$\text{Global Non-Uniformity} = 100 * \left(\frac{\text{Active Area Standard Deviation}}{\text{Active Area Signal}} \right)$$

Units: %rms. Active Area Signal = Active Area Average – Dark Column Average

Global Peak to Peak Non-Uniformity

This test is performed with the imager illuminated to a level such that the output is at 70% of saturation (approximately 924 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 1320 mV. The sensor is partitioned into 256 sub regions of interest, each of which is 128 by 128 pixels in size. The average signal level of each of the 256 sub regions of interest (ROI) is calculated. The signal level of each of the sub regions of interest is calculated using the following formula:

Signal of ROI[i] = (ROI Average in counts – Horizontal overclock average in counts) * mV per count

Where i = 1 to 256. During this calculation on the 144 sub regions of interest, the maximum and minimum signal levels are found. The global peak to peak uniformity is then calculated as:

$$\text{Global Uniformity} = 100 * \frac{\text{Maximum Signal} - \text{Minimum Signal}}{\text{Active Area Signal}}$$

Units: %pp

Center Non-Uniformity

This test is performed with the imager illuminated to a level such that the output is at 70% of saturation (approximately 924 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 1320 mV. Defects are excluded for the calculation of this test. This test is performed on the center 100 by 100 pixels of the sensor. Center uniformity is defined as:

$$\text{Center ROI Uniformity} = 100 * \left(\frac{\text{Center ROI Standard Deviation}}{\text{Center ROI Signal}} \right)$$

Units: %rms. Center ROI Signal = Center ROI Average – Dark Column Average.

Dark Field Defect Test

This test is performed under dark field conditions. The sensor is partitioned into 256 sub regions of interest, each of which is 128 by 128 pixels in size. In each region of interest, the median value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the defect threshold specified in the "Defect Definitions" section.

Bright Field Defect Test

This test is performed with the imager illuminated to a level such that the output is at approximately 924 mV. Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 1320 mV. The average signal level of all active pixels is found. The bright and dark thresholds are set as:

Dark defect threshold = Active Area Signal * threshold

Bright defect threshold = Active Area Signal * threshold

The sensor is then partitioned into 256 sub regions of interest, each of which is 128 by 128 pixels in size. In each region of interest, the average value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the bright threshold specified or if it is less than or equal to the median value of that region of interest minus the dark threshold specified.

- Example for major bright field defective pixels:
- Average value of all active pixels is found to be 924 mV
- Dark defect threshold: 924 mV * 12% = 111 mV
- Bright defect threshold: 924 mV * 12% = 111 mV
- Region of interest #1 selected. This region of interest is pixels 17, 17 to pixels 144, 144
    - Median of this region of interest is found to be 920 mV
    - Any pixel in this region of interest that is ≤ (920 - 111 mV) 809 mV in intensity will be marked defective
    - Any pixel in this region of interest that is ≥ (920 + 111 mV) 1031 mV in intensity will be marked defective
- All remaining 144 sub regions of interest are analyzed for defective pixels in the same manner.

Operation

Absolute Maximum Ratings

Absolute maximum rating is defined as a level or condition that should not be exceeded at any time per the description. If the level or the condition is exceeded, the device will be degraded and may be damaged. Operation at these values will reduce MTTF.

Description	Symbol	Minimum	Maximum	Units	Notes
Operating Temperature	T_{OP}	-50	+70	°C	1
Humidity	RH	+5	+90	%	2
Output Bias Current	I_{out}	-	60	mA	3
Off-chip Load	C_L	-	10	pF	

Notes:
1. Noise performance will degrade at higher temperatures.
2. T=25°C. Excessive humidity will degrade MTTF.
3. Total for all outputs. Maximum current is -15 mA for each output. Avoid shorting output pins to ground or any low impedance source during operation. Amplifier bandwidth increases at higher current and lower load capacitance at the expense of reduced gain (sensitivity).

Absolute Maximum Voltage Ratings Between Pins and Ground

Description	Minimum	Maximum	Units	Notes
VDDα, VOUTα, RDα	-0.4	17.5	V	1
RDα	-0.4	15.5	V	1
V1B, V1T	ESD – 0.4	ESD + 24.0	V	
V2B, V2T, V3B, V3T, V4B, V4T	ESD – 0.4	ESD + 14.0	V	
H1Sα, H1Bα, H2Sα, H2Bα, H2SLα, R1α, R2α, OGα	ESD – 0.4	ESD + 14.0	V	1
ESD	-10.0	0.0	V	
SUB	-0.4	+40.0	V	2

Notes:
1. α denotes a, b, c or d
2. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*

KAI-08050 COMPATIBILITY

The KAI-04070 is pin-for-pin compatible with a camera designed for the KAI-08050 image sensor with the following accommodations:

- To operate in accordance with a system designed for KAI-08050, the target substrate voltage should be set to be 2.0V higher than the value recorded on the KAI-04070 shipping container. This setting will cause the charge capacity to be limited to 20Ke$^-$ (or 660mV).
- On the KAI-04070, pins 17 (R2ab) and 51 (R2cd) should be left floating per the KAI-08050 Device Performance Specification.
- The KAI-04070 will operate in only the high gain mode (33 µV/e).
- All timing and voltages are taken from the KAI-08050 specification sheet.
- The number of horizontal and vertical CCD clock cycles is reduced as appropriate

In addition, if the intent is to operate the KAI-04070 image sensor in a camera designed for the KAI-08050 sensor that has been modified to accept and process the full 40,000 e$^-$ (1,320 mV) output, the following changes to the RD bias must be made:

Pins	Names	KAI-08050	KAI-04070
10, 26, 44, 60	RDa, RDb, RDc, RDd	12.0V per the specification	Increase to 12.6V

To make use of the low or dual gains modes the KAI-04070 voltages and timing specifications must be used.

RESET PIN, LOW GAIN (R2AB AND R2CD)

The R2ab and R2bc (pins 17 and 51) each have an internal circuit to bias the pins to 4.3 V. This feature assures the device is set to operate in the high gain mode when pins 17 and 51 are not connected in the application to a clock driver (for KAI-08050 compatibility). Typical capacitor coupled drivers will not drive this structure.

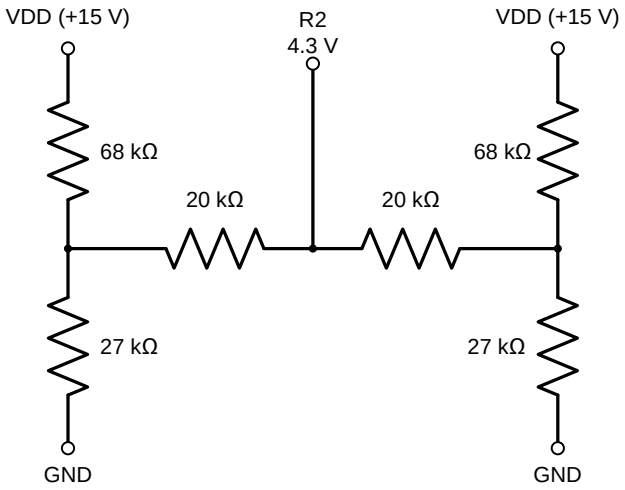


Figure 22: Equivalent Circuit for Reset Gate, low Gain (R2ab and R2cd)

Power-Up and Power-Down Sequence

Adherence to the power-up and power-down sequence is critical. Failure to follow the proper power-up and power-down sequences may cause damage to the sensor.

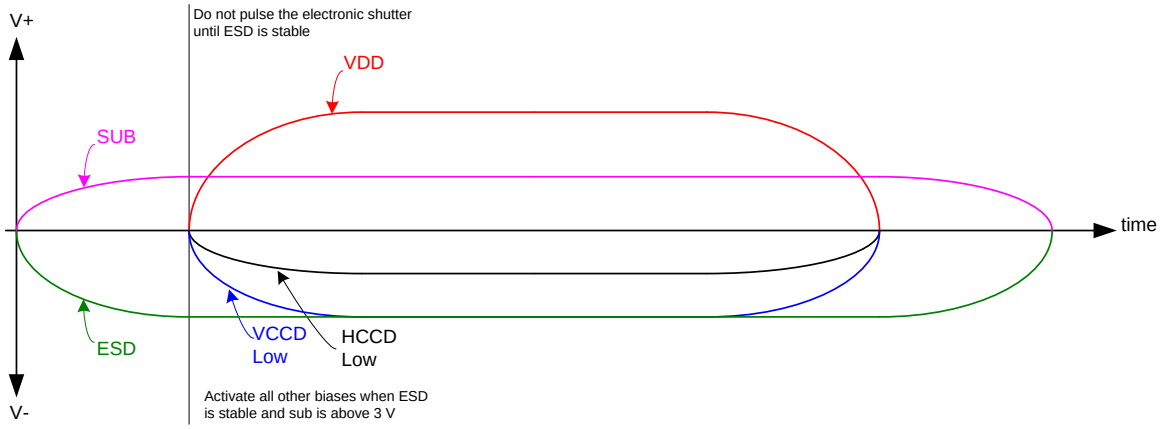
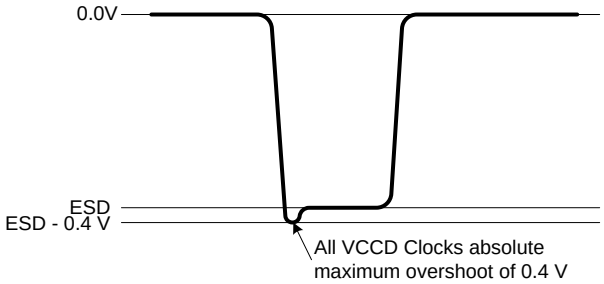


Figure 23: Power-Up and Power-Down Sequence

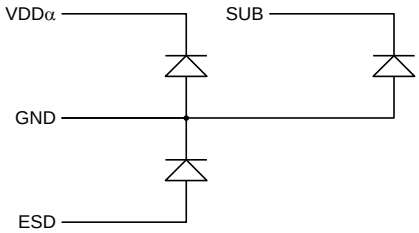
Notes:

1. Activate all other biases when ESD is stable and SUB is above 3V
2. Do not pulse the electronic shutter until ESD is stable
3. VDD cannot be +15V when SUB is 0V
4. The image sensor can be protected from an accidental improper ESD voltage by current limiting the SUB current to less than 10mA. SUB and VDD must always be greater than GND. ESD must always be less than GND. Placing diodes between SUB, VDD, ESD and ground will protect the sensor from accidental overshoots of SUB, VDD and ESD during power on and power off. See the figure below.

The VCCD clock waveform must not have a negative overshoot more than 0.4V below the ESD voltage.



Example of external diode protection for SUB, VDD and ESD. α denotes a, b, c or d.



DC Bias Operating Conditions

Description	Pins	Symbol	Minimum	Nominal	Maximum	Units	Maximum DC Current	Notes
Reset Drain	RDα	RD	+12.4	+12.6	+12.8	V	10 µA	1, 9
Output Gate	OGα	OG	-2.2	-2.0	-1.8	V	10 µA	1
Output Amplifier Supply	VDDα	VDD	+14.5	+15.0	+15.5	V	11.0 mA	1, 2
Ground	GND	GND	0.0	0.0	0.0	V	-1.0 mA	
Substrate	SUB	VSUB	+5.0	VAB	VDD	V	50 µA	3, 8
ESD Protection Disable	ESD	ESD	-9.2	-9.0	Vx_L	V	50 µA	6, 7, 10
Output Bias Current	VOUTα	Iout	-3.0	-5.0	-10.0	mA	——	1, 4, 5

Notes:

1. α denotes a, b, c or d
2. The maximum DC current is for one output. Idd = Iout + Iss. See Figure 24.
3. The operating value of the substrate voltage, VAB, will be marked on the shipping container for each device. The value of VAB is set such that the photodiode charge capacity is the nominal PNe (see Specifications).
4. An output load sink must be applied to each VOUT pin to activate each output amplifier.
5. Nominal value required for 40MHz operation per output. May be reduced for slower data rates and lower noise.
6. Adherence to the power-up and power-down sequence is critical. See Sequence section.
7. ESD maximum value must be less than or equal to V1_L+0.4 V and V2_L+0.4 V.
8. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions.*
9. 12.0 V may be used if the total output signal desired is 20,000 e^- or less.
10. Where Vx_L is the level set for V1_L, V2_L, V3_L, or V4_L in the application.

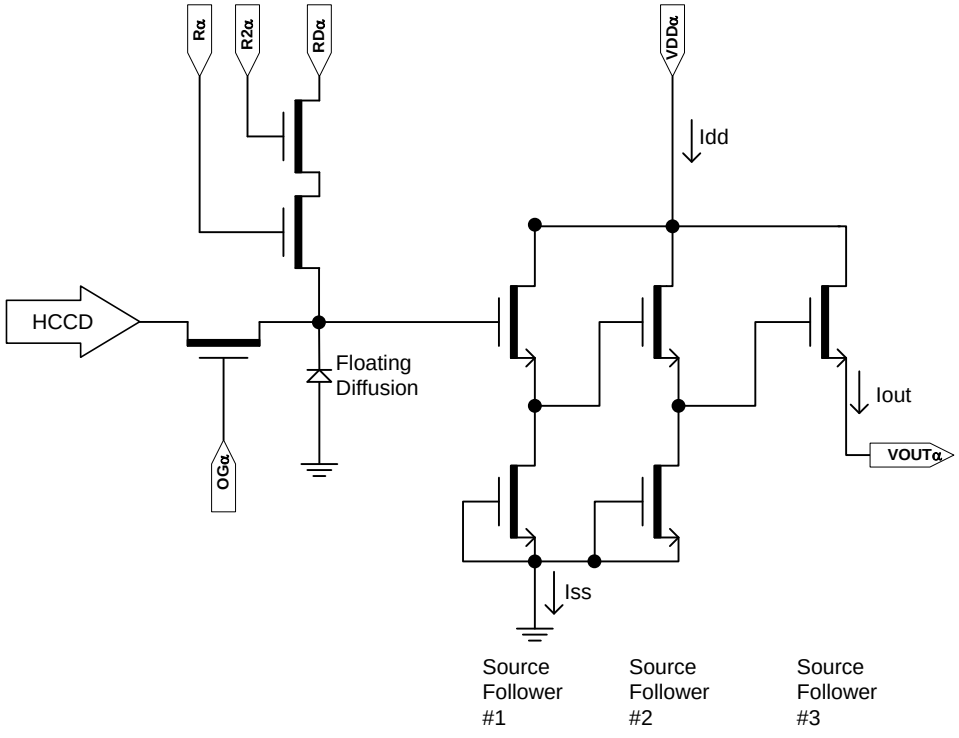


Figure 24: Output Amplifier

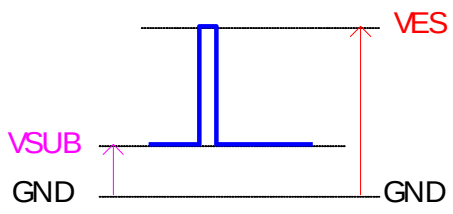
AC Operating Conditions

Clock Levels

Description	Pins[1]	Symbol	Level	Minimum	Nominal	Maximum	Units
Vertical CCD Clock, Phase 1	V1B, V1T	V1_L	Low	-8.2	-8.0	-7.8	V
		V1_M	Mid	-0.2	+0.0	+0.2	
		V1_H	High	11.5	12.0	12.5	
Vertical CCD Clock, Phase 2	V2B, V2T	V2_L	Low	-8.2	-8.0	-7.8	V
		V2_H	High	-0.2	+0.0	+0.2	
Vertical CCD Clock, Phase 3	V3B, V3T	V3_L	Low	-8.2	-8.0	-7.8	V
		V3_H	High	-0.2	+0.0	+0.2	
Vertical CCD Clock, Phase 4	V4B, V4T	V4_L	Low	-8.2	-8.0	-7.8	V
		V4_H	High	-0.2	+0.0	+0.2	
Horizontal CCD Clock, Phase 1 Storage	H1Sα	H1S_L	Low	-5.2	-4.0	-3.8	V
		H1S_A	Amplitude[3]	+3.8	+4.0	+5.2	
Horizontal CCD Clock, Phase 1 Barrier	H1Bα	H1B_L	Low	-5.2	-4.0	-3.8	V
		H1B_A	Amplitude[3]	+3.8	+4.0	+5.2	
Horizontal CCD Clock, Phase 2 Storage	H2Sα	H2S_L	Low	-5.2	-4.0	-3.8	V
		H2S_A	Amplitude[3]	+3.8	+4.0	+5.2	
Horizontal CCD Clock, Phase 2 Barrier	H2Bα	H2B_L	Low	-5.2	-4.0	-3.8	V
		H2B_A	Amplitude[3]	+3.8	+4.0	+5.2	
Horizontal CCD Clock, Last Phase[2]	H2SLα	H2SL_L	Low	-5.2	-5.0	-4.8	V
		H2SL_A	Amplitude[3]	+4.8	+5.0	+5.2	
Reset Gate	Rα	R_L	Low	-3.2	-3.0	-2.8	V
		R_A	Amplitude	+6.0	———	+6.4	
Reset Gate 2	R2α	R2_L	Low	-2.0	-1.8	-1.6	V
		R2_A	Amplitude	+6.0	———	+6.4	
Electronic Shutter[4]	SUB	VES	High	+29.0	+30.0	+40.0	V

Notes:
1. α denotes a, b, c or d
2. Use separate clock driver for improved speed performance.
3. The horizontal clock amplitude should be set such that the high level reaches 0.0 volts. Examples:
   a. If the minimum horizontal low voltage of -5.2V is used, then a 5.2 volt amplitude clock is required for a clock swing of -5.2V to 0.0V
   b. If the maximum horizontal low voltage of -3.8V is used, then a 3.8 volt amplitude clock is required for a clock swing of -3.8V to 0.0V
4. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*

The figure below shows the DC bias (VSUB) and AC clock (VES) applied to the SUB pin. Both the DC bias and AC clock are referenced to ground.



Capacitance

	V1B	V2B	V3B	V4B	V1T	V2T	V3T	V4T	GND	All Pins	Units
V1B		4	3	3	2	2	2	1	10	25	nF
V2B			1	3	1	1	1	1	10	20	nF
V3B				5	2	1	2	1	6	23	nF
V4B					2	1	1	1	13	23	nF
V1T						2	3	2	20	29	nF
V2T							5	3	4	21	nF
V3T								2	9	24	nF
V4T									3	20	nF
VSub	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	2.8	2.8	nF

	H2S	H1B	H2B	GND	All Pins	Units
H1S	32	29	29	120	210	pF
H2S		16	21	170	240	pF
H1B			7	155	210	pF
H2B				165	235	pF

Notes
1. Tables show typical cross capacitance between pins of the device
2. Capacitance is total for all like pins
3. Capacitance values are estimated

DEVICE IDENTIFICATION

The device identification pin (DevID) may be used to determine which Truesense Imaging 7.4 micron pixel interline CCD sensor is being used.

Description	Pins	Symbol	Minimum	Nominal	Maximum	Units	Maximum DC Current	Notes
Device Identification	DevID	DevID	64,000	74,000	84,000	Ohms	50 µA	1, 2, 3

Notes:
1. Nominal value subject to verification and/or change during release of preliminary specifications.
2. If the Device Identification is not used, it may be left disconnected.
3. After Device Identification resistance has been read during camera initialization, it is recommended that the circuit be disabled to prevent localized heating of the sensor due to current flow through the R_DeviceID resistor.

Recommended Circuit

Note that V1 must be a different value than V2.

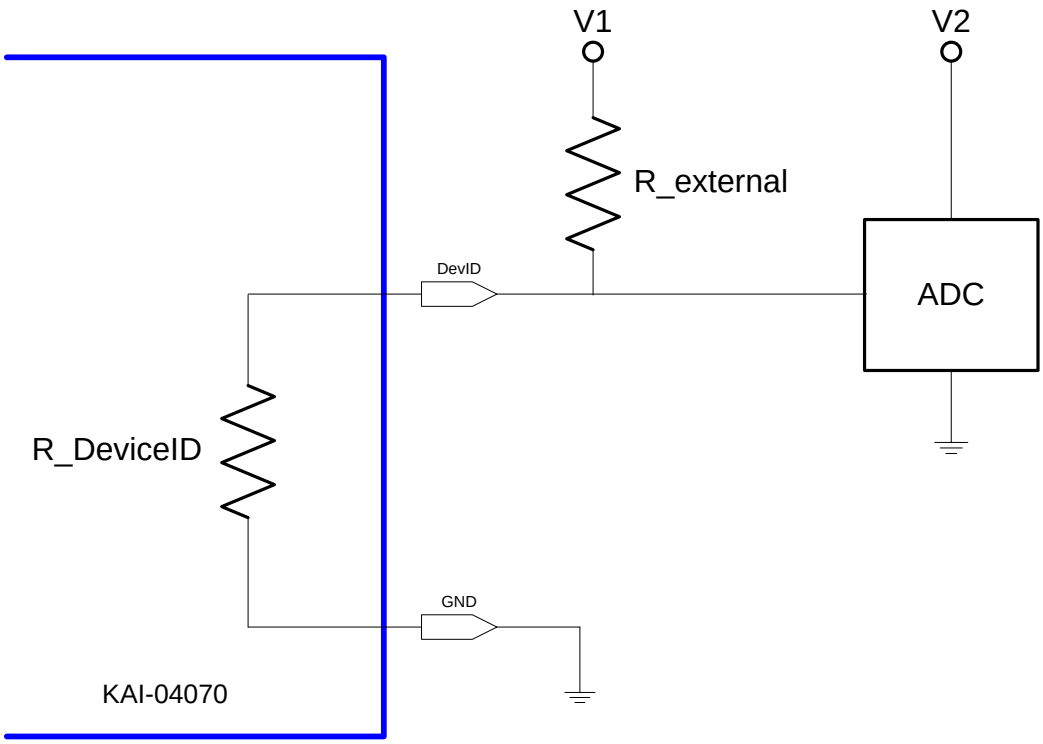


Figure 25: Device Identification Recommended Circuit

Timing

Requirements and Characteristics

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
Photodiode Transfer	Tpd	1.0	-	-	µs	
VCCD Leading Pedestal	T3p	4.0	-	-	µs	
VCCD Trailing Pedestal	T3d	4.0	-	-	µs	
VCCD Transfer	Tv	2.0	-	-	µs	
VCCD Clock Cross-over	Vvcr	75	-	100	%	1
VCCD Rise, Fall Times	Tvr, Tvf	5	-	10	%	1, 2
HCCD Delay	Ths	2.0	-	-	µs	
HCCD Transfer	Te	25.0	-	-	ns	
Shutter Transfer	Tsub	2.0	-	-	µs	
Shutter Delay	Thd	2.0	-	-	µs	
Reset Pulse	Tr	2.5	-	-	ns	
Reset – Video Delay	Trv	-	2.2	-	ns	
H2SL – Video Delay	Thv	-	3.1	-	ns	
Line Time	Tline	34.9	-	-	µs	Dual HCCD Readout
		61.5	-	-		Single HCCD Readout
Frame Time	Tframe	36.9	-	-	ms	Quad HCCD Readout
		73.8	-	-		Dual HCCD Readout
		129.9	-	-		Single HCCD Readout
Line Time (XLDR Bin 2x2)	Tline	69.8	-	-	µs	Dual HCCD Readout
		123.0	-	-		Single HCCD Readout
Frame Time (XLDR Bin 2x2) Constant HCCD timing	Tframe	36.9	-	-	ms	Quad HCCD Readout
		73.7	-	-		Dual HCCD Readout
		129.9	-	-		Single HCCD Readout
Frame Time (XLDR Bin 2x2) Variable HCCD timing	Tframe	29.8	-	-	ms	Quad HCCD Readout
		59.5	-	-		Dual HCCD Readout
		101.7	-	-		Single HCCD Readout

Notes:
1. Refer to Figure 43: VCCD Clock Rise Time, Fall Time, and Edge Alignment
2. Relative to the VCCD Transfer pulse width, Tv

TIMING FLOW CHARTS

In the timing flow charts the number of HCCD clock cycles per row, NH, and the number of VCCD clock cycles per frame, NV, are shown in the following table

	Full Resolution		1/4 Resolution		XLDR	
	NV	NH	NV	NH	NV	NH
Quad	1056	1076	528	538	528	538
Dual VOUTa, VOUTc	1056	2152	528	1076	528	1076
Dual VOUTa, VOUTb	2112	1076	1056	538	1056	538
Single VOUTa	2112	2152	1056	1076	1056	1076

Table 1: Values for NH and NV When Operating the Sensor in the Various Modes of Resolution

Notes:

1. The time to read out one line Tline = Line Timing + NH / (pixel frequency).
2. The time to read out one frame Tframe = NV * Tline + Frame Timing.
3. Line Timing: See Table 3: Line Timing.
4. Frame Timing: See Table 2: Frame Timing.
5. XLDR: eXtended Linear Dynamic Range.

No Electronic Shutter

In this case the photodiode exposure time is equal to the time to read out an image. This flow chart applies to both full and1/4 resolution modes.

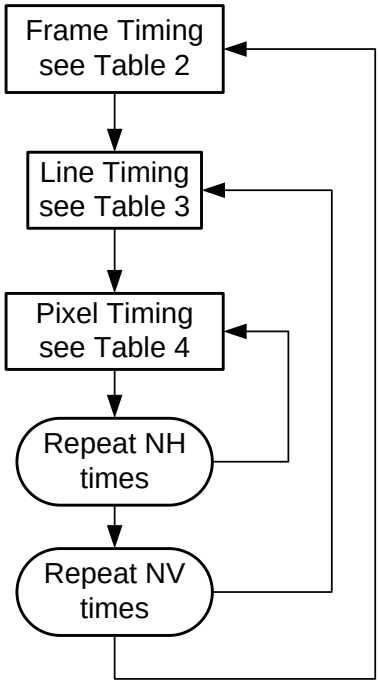


Figure 26: Timing Flow When Electronic Shutter is Not Used

Using the Electronic Shutter

This flow chart applies to both the full and 1/4 resolution modes. The exposure time begins on the falling edge of the electronic shutter pulse on the SUB pin. The exposure time ends on the falling edge of the photodiode transfer (Tpd) of the V1T and V1B pins. The electronic shutter timing is shown in Figure.

NEXP: Exposure time in increments of number of lines.

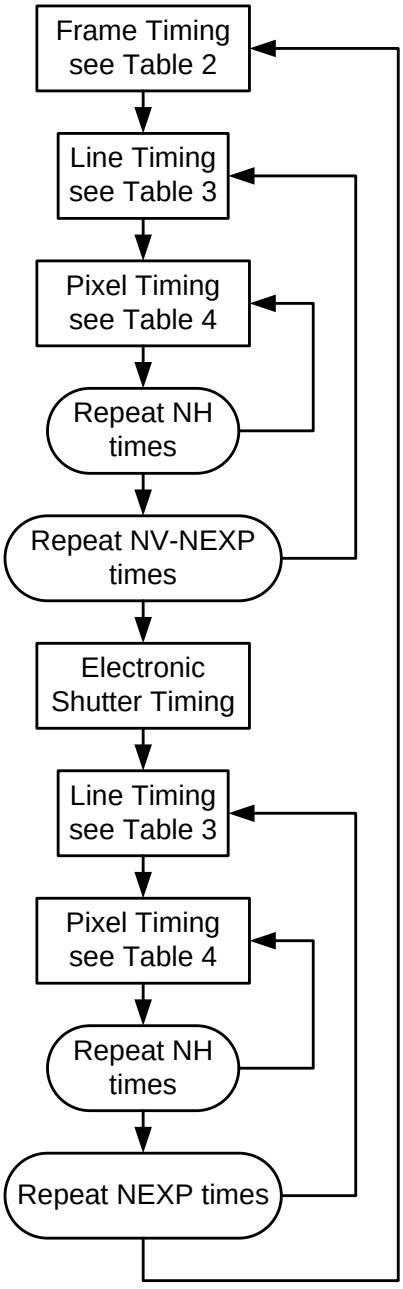


Figure 27: Timing Flow Chart Using the Electronic Shutter for Exposure Control

TIMING TABLES

Frame Timing

This timing table is for transferring charge from the photodiodes to the VCCD. See Figure 28 and Figure 29 for frame timing diagrams.

	Full Resolution, high gain OR low gain				1/4 Resolution, high gain OR low gain				1/4 Resolution XLDR			
Device Pin	Quad	Dual VOUTa VOUTc	Dual VOUTa VOUTb	Single VOUTa	Quad	Dual VOUTa VOUTc	Dual VOUTa VOUTb	Single VOUTa	Quad	Dual VOUTa VOUTc	Dual VOUTa VOUTb	Single VOUTa
V1T	F1T		F1B	F1B	F1T		F1B		F1T		F1B	
V2T	F2T		F4B	F4B	F2T		F4B		F2T		F4B	
V3T	F3T		F3B	F3B	F3T		F3B		F3T		F3B	
V4T	F4T		F2B	F2B	F4T		F2B		F4T		F2B	
V1B	F1B				F1B				F1B			
V2B	F2B				F2B				F2B			
V3B	F3B				F3B				F3B			
V4B	F4B				F4B				F4B			
H1Sa	P1				P1Q				P1XL			
H1Ba	P1				P1Q				P1XL			
H2Sa	P2				P2Q				P2XL			
H2Ba	P2				P2Q				P2XL			
Ra	RHG/RLG				RHGQ/RLGQ				RXL			
H1Sb	P1				P1Q				P1XL			
H1Bb	P1	P2	P1	P2	P1Q	P2Q	P1Q	P2Q	P1XL	P2XL	P1XL	P2XL
H2Sb	P2				P2Q				P2XL			
H2Bb	P2	P1	P2	P1	P2Q	P1Q	P2Q	P1Q	P2XL	P1XL	P2XL	P1XL
Rb	RHG/RLG	Note 1	RHG/RLG	Note 1	RHGQ/RLGQ	Note 1	RHGQ/RLGQ	Note 1	RXL	Note 1	RXL	Note 1
R2ab	R2HG/R2LG				R2HGQ/R2LGQ				R2XL			
H1Sc	P1		Note 1		P1Q		Note 1		P1XL		Note 1	
H1Bc	P1		Note 1		P1Q		Note 1		P1XL		Note 1	
H2Sc	P2		Note 1		P2Q		Note 1		P2XL		Note 1	
H2Bc	P2		Note 1		P2Q		Note 1		P2XL		Note 1	
Rc	RHG/RLG		Note 1		RHGQ/RLGQ		Note 1		RXL		Note 1	
H1Sd	P1		Note 1		P1Q		Note 1		P1XL		Note 1	
H1Bd	P1	P2	Note 1		P1Q	P2Q	Note 1		P1XL	P2XL	Note 1	
H2Sd	P2		Note 1		P2Q		Note 1		P2XL		Note 1	
H2Bd	P2	P1	Note 1		P2Q	P1Q	Note 1		P2XL	P1XL	Note 1	
Rd	RHG/RLG	Note 1			RHGQ/RLGQ	Note 1			RXL	Note 1		
R2cd	R2HG/R2LG		Note 1		R2HGQ/R2LGQ		Note 1		R2XL		Note 1	
SHP (2)	SHP1				SHPQ				Note 4			
SHD (2)	SHD1				SHDQ				Note 5			

Table 2: Frame Timing

Notes:

1. This clock should be held at its high level voltage (0V) or held at +5.0V for compatibility with TRUESENSE 5.5 micron Interline Transfer CCD family of products
2. SHP and SHD are the sample clocks for the analog front end (AFE) signal processor
3. This note intentionally left empty
4. Use SHPLG for the AFE processing the low gain signal. Use SHPHG for the AFE processing the high gain signal
5. Use SHDLG for the AFE processing the low gain signal. Use SHDHG for the AFE processing the high gain signal

Line Timing

This timing is for transferring one line of charge from the VCCD to the HCCD. See Figure 30, Figure 31, Figure 32 and Figure 33 for line timing diagrams.

	Full Resolution, high gain OR low gain				1/4 Resolution, high gain OR low gain				1/4 Resolution XLDR			
Device Pin	Quad	Dual VOUTa VOUTc	Dual VOUTa VOUTb	Single VOUTa	Quad	Dual VOUTa VOUTc	Dual VOUTa VOUTb	Single VOUTa	Quad	Dual VOUTa VOUTc	Dual VOUTa VOUTb	Single VOUTa
V1T	L1T		L1B		2x L1T		2x L1B		2x L1T		2x L1B	
V2T	L2T		L4B		2x L2T		2x L4B		2x L2T		2x L4B	
V3T	L3T		L3B		2x L3T		2x L3B		2x L3T		2x L3B	
V4T	L4T		L2B		2x L4T		2x L2B		2x L4T		2x L2B	
V1B	L1B				2x L1B				2x L1B			
V2B	L2B				2x L2B				2x L2B			
V3B	L3B				2x L3B				2x L3B			
V4B	L4B				2x L4B				2x L4B			
H1Sa	P1L				P1LQ				P1XL			
H1Ba	P1L				P1LQ				P1XL			
H2Sa	P2L				P2LQ				P2XL			
H2Ba	P2L				P2LQ				P2XL			
Ra	RHG/RLG				RHGQ/RLGQ				RXL			
H1Sb	P1L				P1LQ				P1XL			
H1Bb	P1L	P2L	P1L	P2L	P1LQ	P2LQ	P1LQ	P2LQ	P1XL	P2XL	P1XL	P2XL
H2Sb	P2L				P2LQ				P2XL			
H2Bb	P2L	P1L	P2L	P1L	P2LQ	P1LQ	P2LQ	P1LQ	P2XL	P1XL	P2XL	P1XL
Rb	RHG/RLG	Note 1	RHG/RLG	Note 1	RHGQ/RLGQ	Note 1	RHGQ/RLGQ	Note 1	RXL	Note 1	RXL	Note 1
R2ab	R2HG/R2LG				R2HGQ/R2LGQ				R2XL			
H1Sc	P1L		Note 1		P1LQ		Note 1		P1XL		Note 1	
H1Bc	P1L		Note 1		P1LQ		Note 1		P1XL		Note 1	
H2Sc	P2L		Note 1		P2LQ		Note 1		P2XL		Note 1	
H2Bc	P2L		Note 1		P2LQ		Note 1		P2XL		Note 1	
Rc	RHG/RLG		Note 1		RHGQ/RLGQ		Note 1		RXL		Note 1	
H1Sd	P1L		Note 1		P1LQ		Note 1		P1XL		Note 1	
H1Bd	P1L	P2L	Note 1		P1LQ	P2LQ	Note 1		P1XL	P2XL	Note 1	
H2Sd	P2L		Note 1		P2LQ		Note 1		P2XL		Note 1	
H2Bd	P2L	P1L	Note 1		P2LQ	P1LQ	Note 1		P2XL	P1XL	Note 1	
Rd	RHG/RLG	Note 1			RHGQ/RLGQ	Note 1			RXL	Note 1		
R2cd	R2HG/R2LG		Note 1		R2HGQ/R2LGQ		Note 1		R2XL		Note 1	
SHP (2)	SHP1				SHPQ				Note 4			
SHD (2)	SHD1				SHDQ				Note 5			

Table 3: Line Timing

Notes:

1. This clock should be held at its high level voltage (0V) or held at +5.0V for compatibility with TRUESENSE 5.5 micron Interline Transfer CCD family of products
2. SHP and SHD are the sample clocks for the analog front end (AFE) signal processor
3. The notation 2x L1B means repeat the L1B timing twice for every line. This sums two rows into the HCCD.
4. Use SHPLG for the AFE processing the low gain signal. Use SHPHG for the AFE processing the high gain signal
5. Use SHDLG for the AFE processing the low gain signal. Use SHDHG for the AFE processing the high gain signal

Pixel Timing

This timing is for transferring one pixel from the HCCD to the output amplifier.

	Full Resolution, high gain OR low gain				1/4 Resolution, high gain OR low gain				1/4 Resolution XLDR			
Device Pin	Quad	Dual VOUTa VOUTc	Dual VOUTa VOUTb	Single VOUTa	Quad	Dual VOUTa VOUTc	Dual VOUTa VOUTb	Single VOUTa	Quad	Dual VOUTa VOUTc	Dual VOUTa VOUTb	Single VOUTa
V1T	-8V				-8V				-8V			
V2T	-8V				-8V				-8V			
V3T	0V				0V				0V			
V4T	0V				0V				0V			
V1B	-8V				-8V				-8V			
V2B	0V				0V				0V			
V3B	0V				0V				0V			
V4B	-8V				-8V				-8V			
H1Sa	P1				P1Q				P1XL			
H1Ba	P1				P1Q				P1XL			
H2Sa	P2				P2Q				P2XL			
H2Ba	P2				P2Q				P2XL			
Ra	RHG/RLG				RHGQ/RLGQ				RXL			
H1Sb	P1				P1Q				P1XL			
H1Bb	P1	P2	P1	P2	P1Q	P2Q	P1Q	P2Q	P1XL	P2XL	P1XL	P2XL
H2Sb	P2				P2Q				P2XL			
H2Bb	P2	P1	P2	P1	P2Q	P1Q	P2Q	P1Q	P2XL	P1XL	P2XL	P1XL
Rb	RHG/RLG	Note 1	RHG/RLG	Note 1	RHGQ/RLGQ	Note 1	RHGQ/RLGQ	Note 1	RXL	Note 1	RXL	Note 1
R2ab	R2HG/R2LG				R2HGQ/R2LGQ				R2XL			
H1Sc	P1		Note 1		P1Q		Note 1		P1XL		Note 1	
H1Bc	P1		Note 1		P1Q		Note 1		P1XL		Note 1	
H2Sc	P2		Note 1		P2Q		Note 1		P2XL		Note 1	
H2Bc	P2		Note 1		P2Q		Note 1		P2XL		Note 1	
Rc	RHG/RLG		Note 1		RHGQ/RLGQ		Note 1		RXL		Note 1	
H1Sd	P1		Note 1		P1Q		Note 1		P1XL		Note 1	
H1Bd	P1	P2	Note 1		P1Q	P2Q	Note 1		P1XL	P2XL	Note 1	
H2Sd	P2		Note 1		P2Q		Note 1		P2XL		Note 1	
H2Bd	P2	P1	Note 1		P2Q	P1Q	Note 1		P2XL	P1XL	Note 1	
Rd	RHQ/RLG	Note 1			RHGQ/RLGQ	Note 1			RXL	Note 1		
R2cd	R2HG/R2LG		Note 1		R2HGQ/R2LGQ		Note 1		R2XL		Note 1	
SHP (2)	SHP1				SHPQ				Note 4			
SHD (2)	SHD1				SHDQ				Note 5			

Table 4: Pixel Timing

Notes:

1. This clock should be held at its high level voltage (0V) or held at +5.0V for compatibility with TRUESENSE 5.5 micron Interline Transfer CCD family of products
2. SHP and SHD are the sample clocks for the analog front end (AFE) signal processor
3. This note intentionally left empty
4. Use SHPLG for the AFE processing the low gain signal. Use SHPHG for the AFE processing the high gain signal
5. Use SHDLG for the AFE processing the low gain signal. Use SHDHG for the AFE processing the high gain signal

TIMING DIAGRAMS

The charge in the photodiodes its transfer to the VCCD on the rising edge of the +12V pulse and is completed by the falling edge of the +12V pulsed on F1T and F1B. During the time period when F1T and F1B are at +12V (Tpd) antiblooming protection is disabled. The photodiode integration time ends on the falling edge of the +12V pulse.

See Table for pin assignments.

Frame Timing – Quadrant and Dual VOUTa/VOUTc Readout Modes

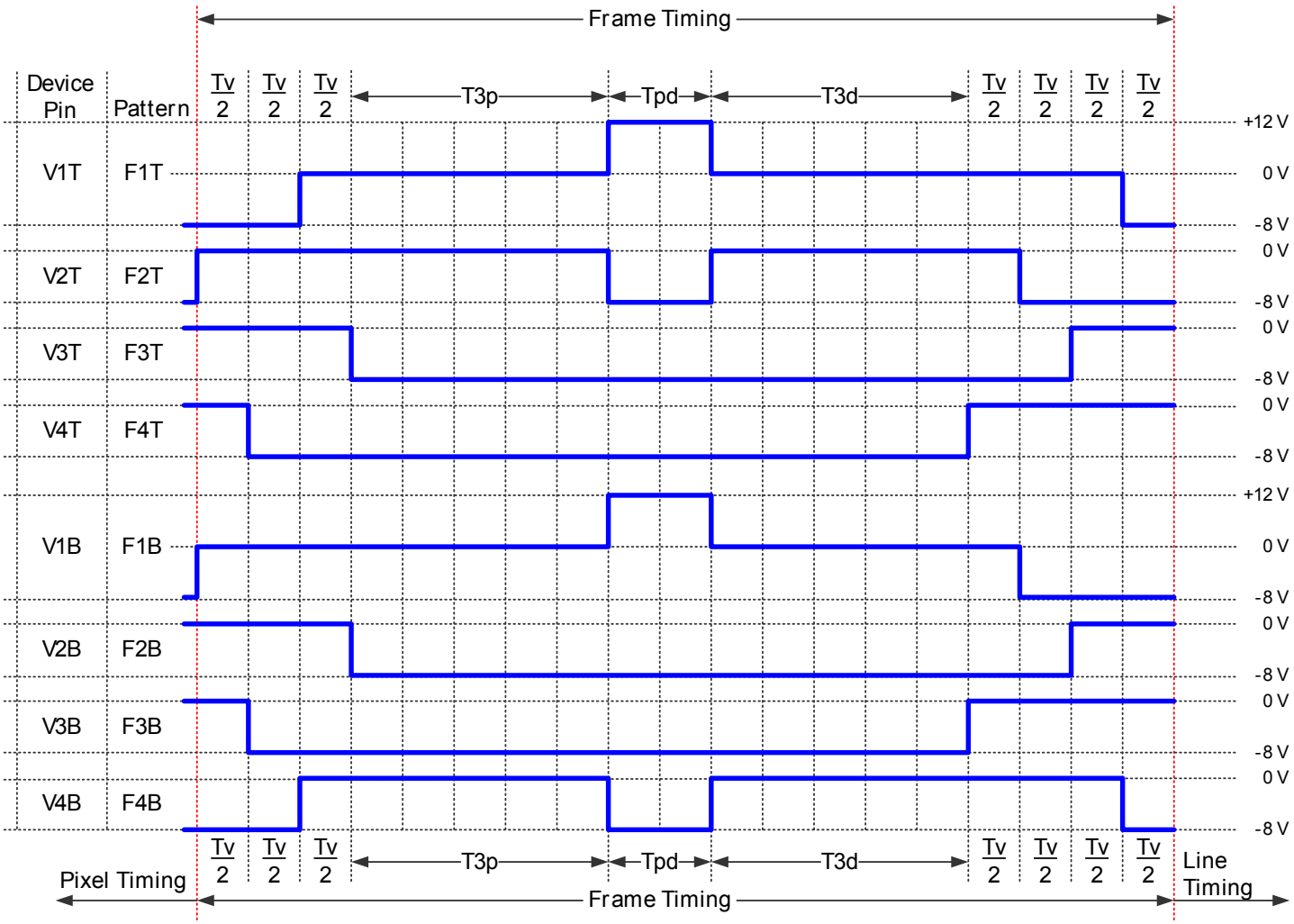


Figure 28: Frame Timing Diagram Quadrant and Dual VOUTa/VOUTc Readout Modes

Frame Timing – Single and Dual VOUTa/VOUTb Readout Modes

See Table 2for pin assignments.

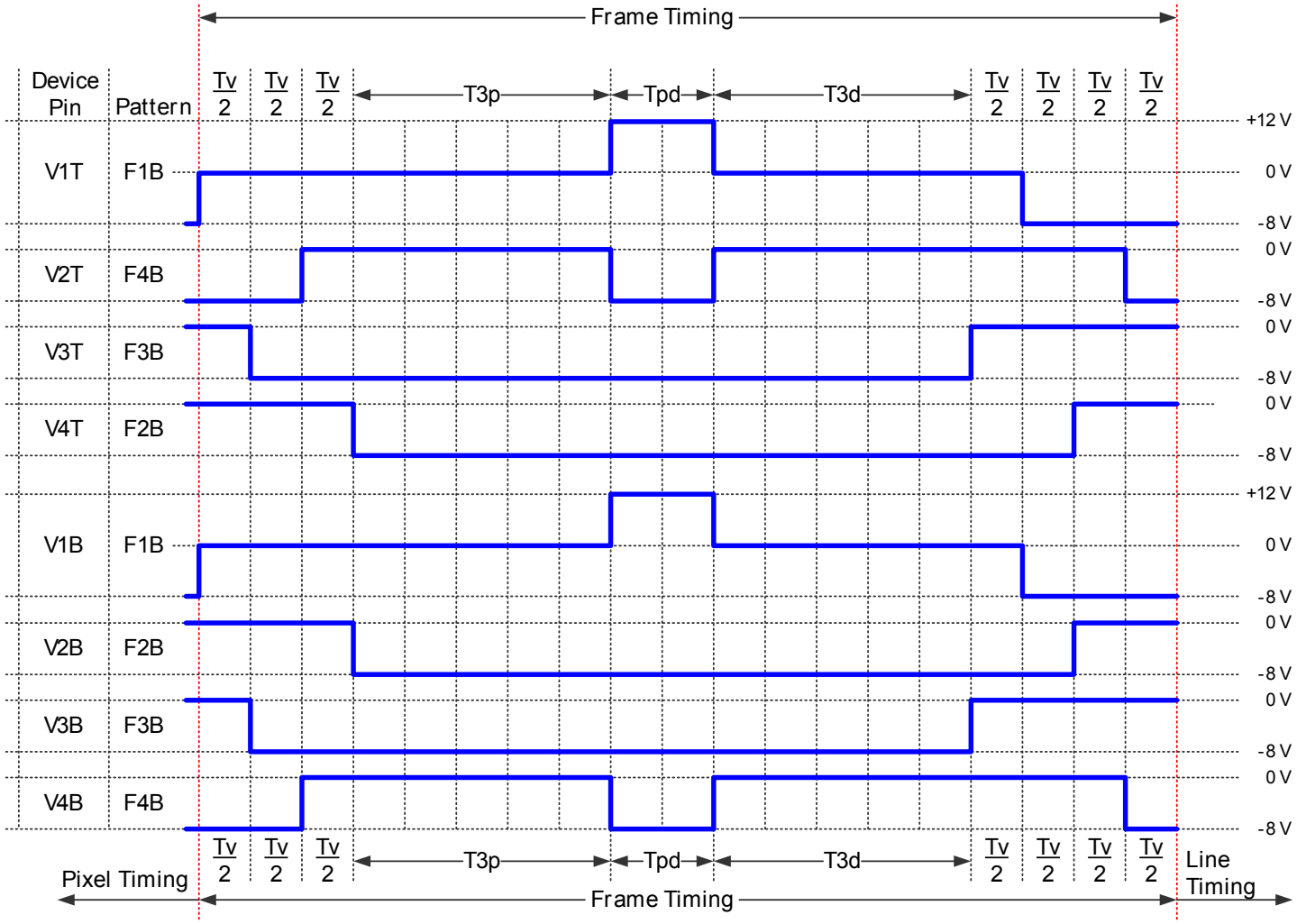


Figure 29: Frame Timing Diagram Single and Dual VOUTa/VOUTb Readout Modes

Line Timing – Full Resolution – Quadrant and Dual VOUTa/VOUTc Readout Modes

See Table for device pin assignments.

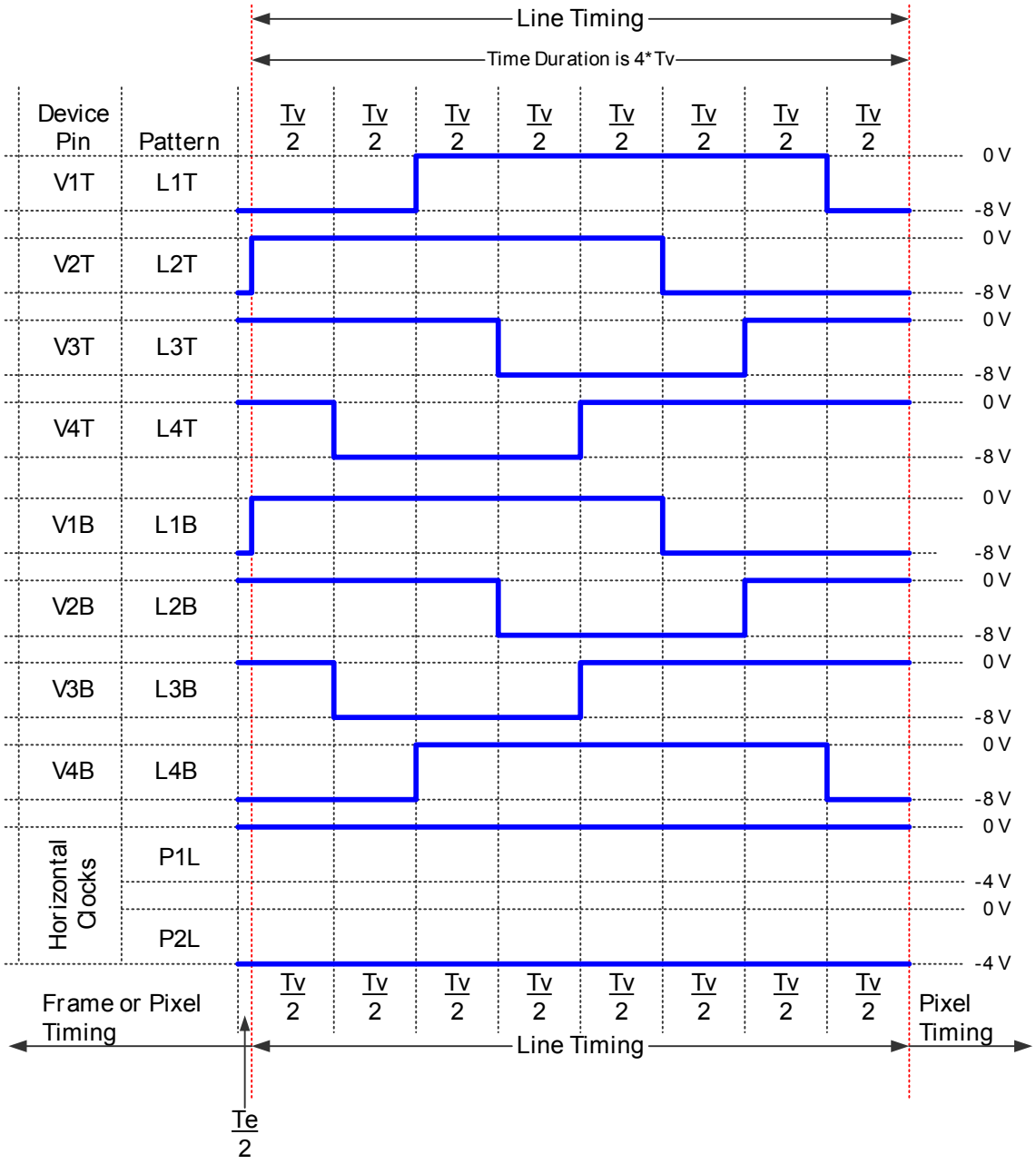


Figure 30: Line Timing Diagram – Full Resolution – Quadrant and Dual VOUTa/VOUTc Modes

Line Timing – Full Resolution – Single and Dual VOUTa/VOUTb Readout Modes

See Table 3for device pin assignments.

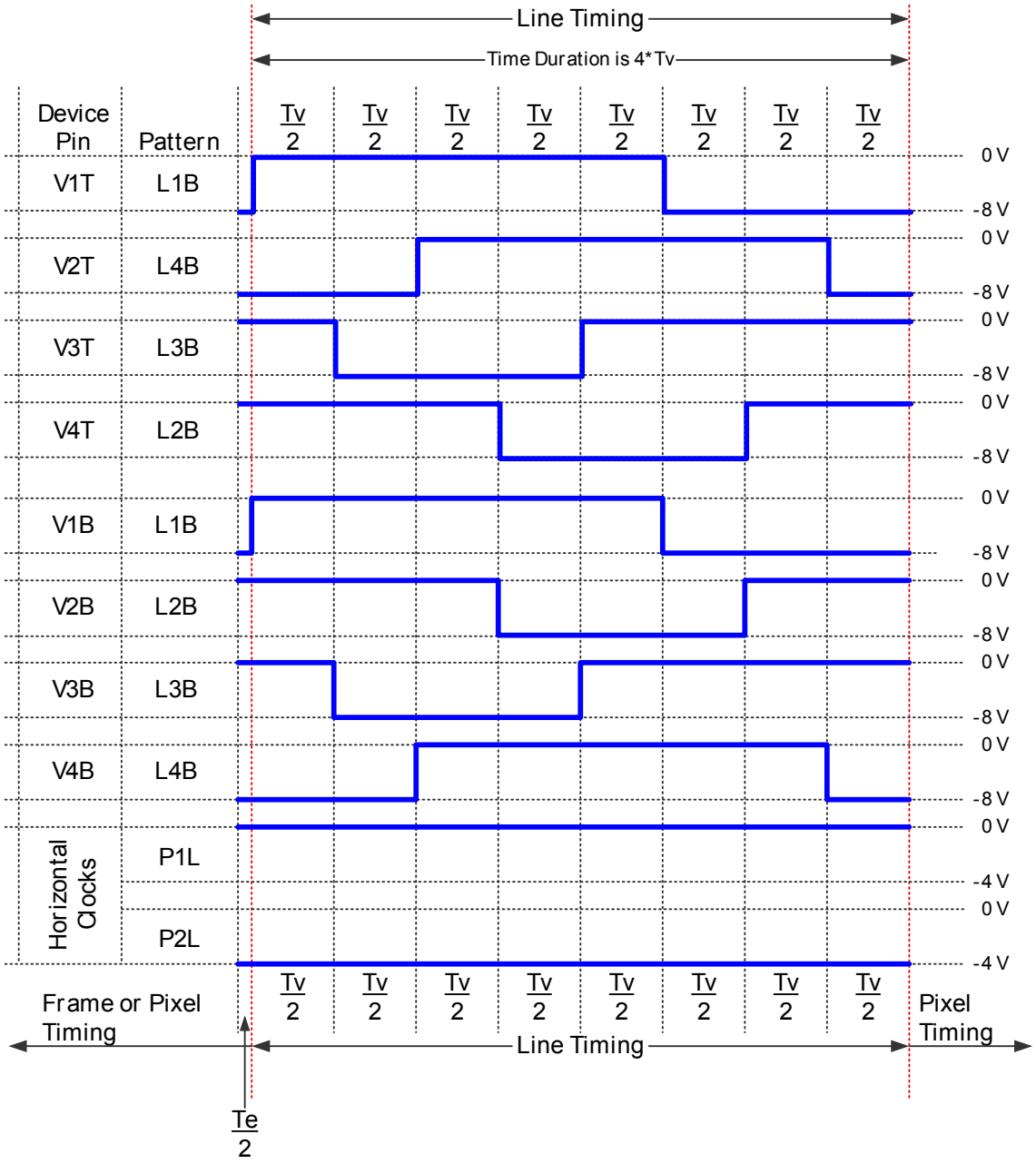


Figure 31: Line Timing Diagram – Full Resolution – Single and Dual VOUTa/VOUTb Modes

Line Timing – Low Gain, High Gain and XLDR 1/4 Resolution – Quadrant and Dual VOUTa/VOUTc Readout Modes

See Table 3for device pin assignments

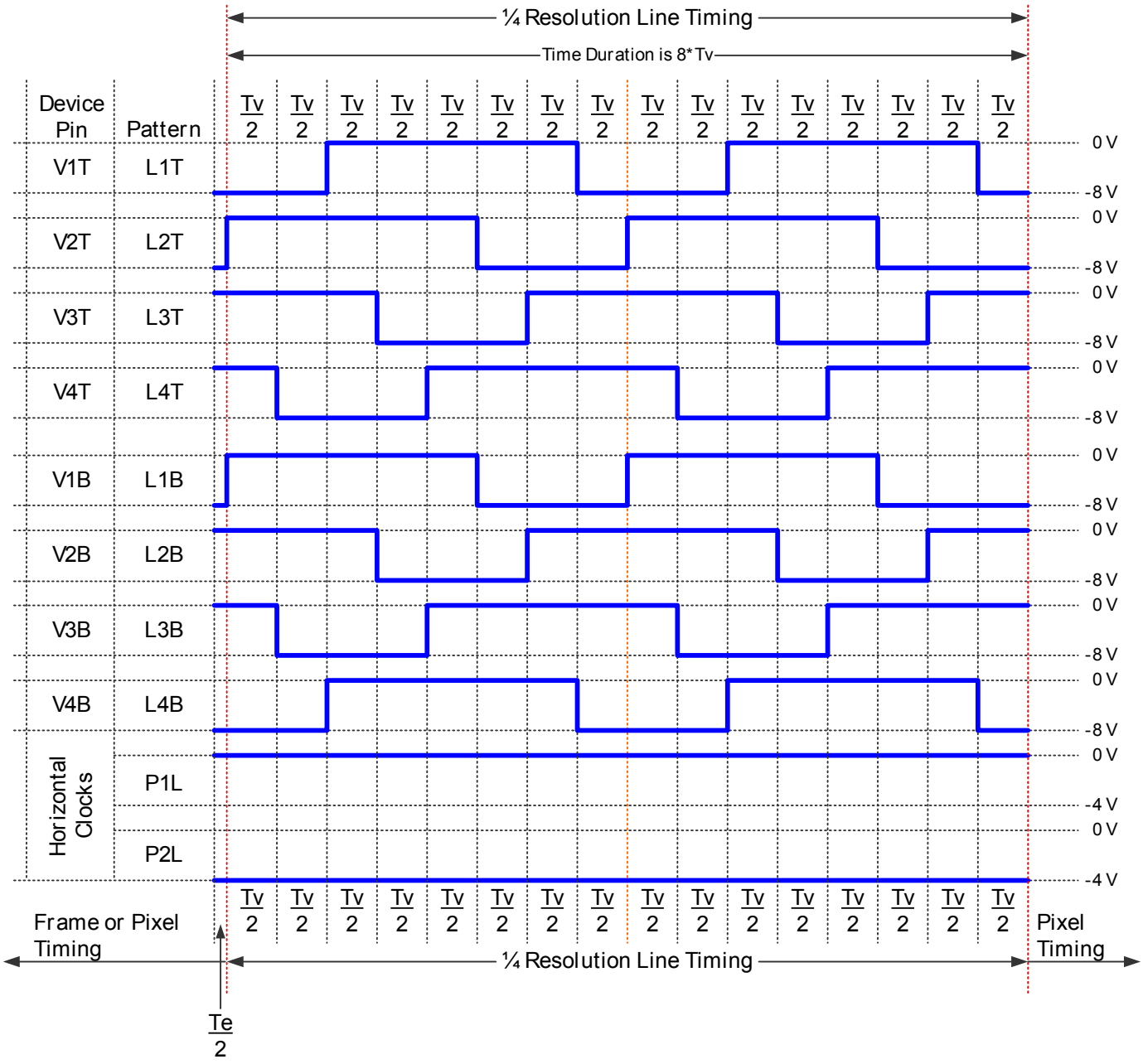


Figure 32: Line Timing Diagram – 1/4 Resolution – Quadrant and Dual VOUTa/VOUTc Modes

Line Timing – Low Gain, High Gain and XLDR 1/4 Resolution – Single and Dual VOUTa/VOUTb Readout Modes

See Table 3for device pin assignments

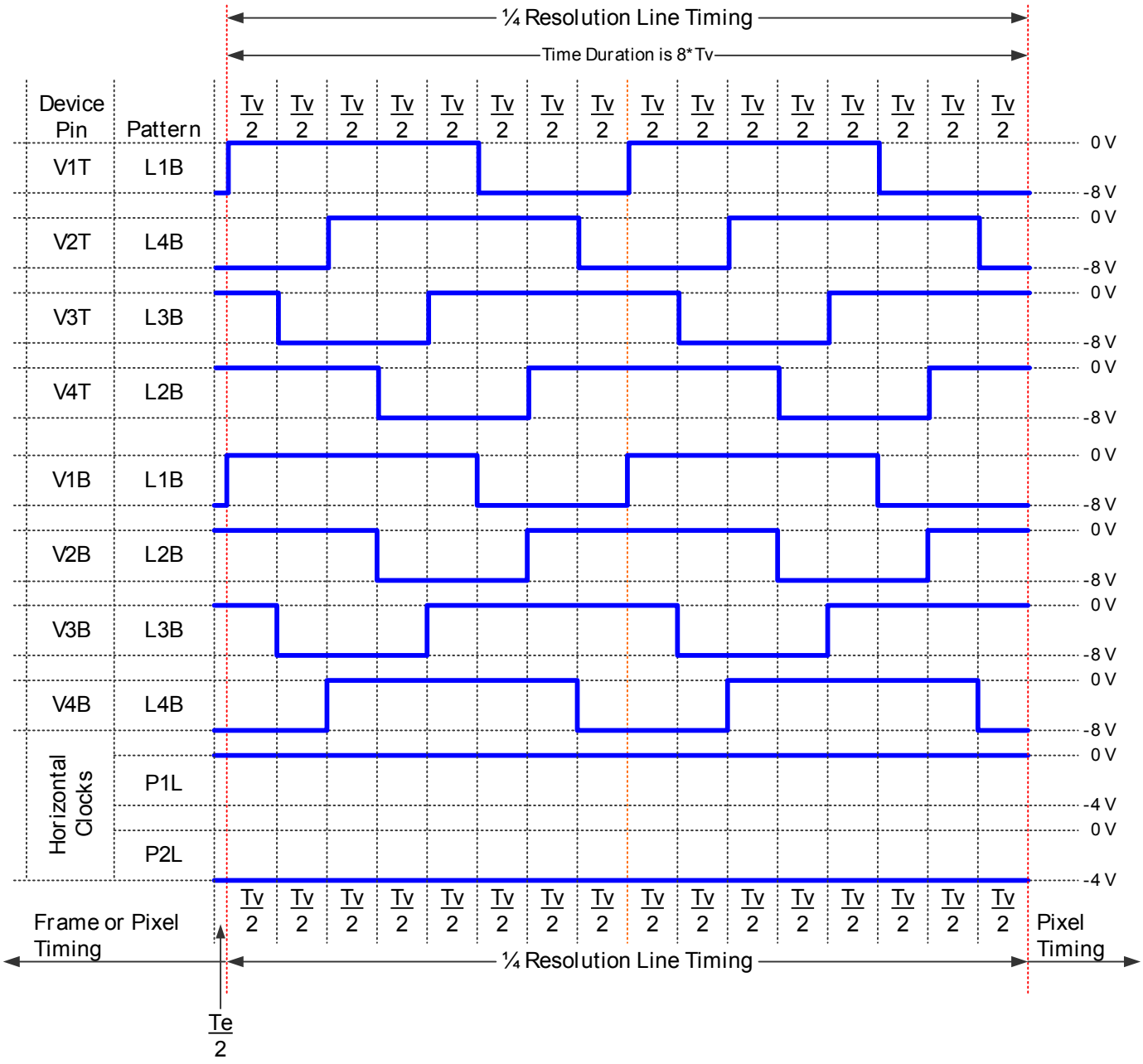


Figure 33: Line Timing Diagram – 1/4 Resolution – Single and Dual VOUTa/VOUTb Modes

Electronic Shutter Timing Diagrams

The electronic shutter pulse can be inserted at the end of any line of the HCCD timing. The HCCD should be empty when the electronic shutter is pulsed. A recommended position for the electronic shutter is just after the last pixel is read out of a line. The VCCD clocks should not resume until at least Tv/2 after the electronic shutter pulse has finished. The HCCD clocks can be run during the electronic shutter pulse as long as the HCCD does not contain valid image data.

For short exposures less than one line time, the electronic shutter pulse can appear inside the frame timing. Any electronic shutter pulse transition should be Tv/2 away from any VCCD clock transition.

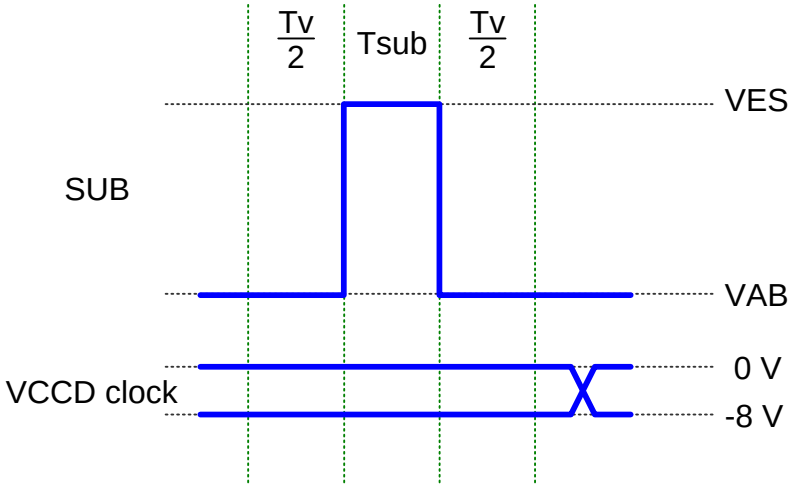


Figure 34: Electronic Shutter Timing

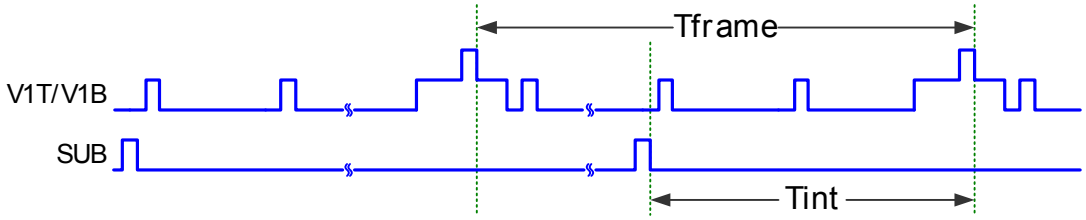


Figure 35: Frame/Electronic Shutter Timing

Pixel Timing – Full Resolution – High Gain Pixel Timing

Use this timing to read out every pixel at high gain. If the sensor is to be permanently operated at high gain, the R2ab and R2cd pins can be left floating or set to any DC voltage between +3V and +5V. Note the R2ab and R2cd pins are internally biased to +4.3V when left floating. The SHP1 and SHD1 pulses indicate where the camera electronics should sample the video waveform. The SHP1 and SHD1 pulses are not applied to the image sensor.

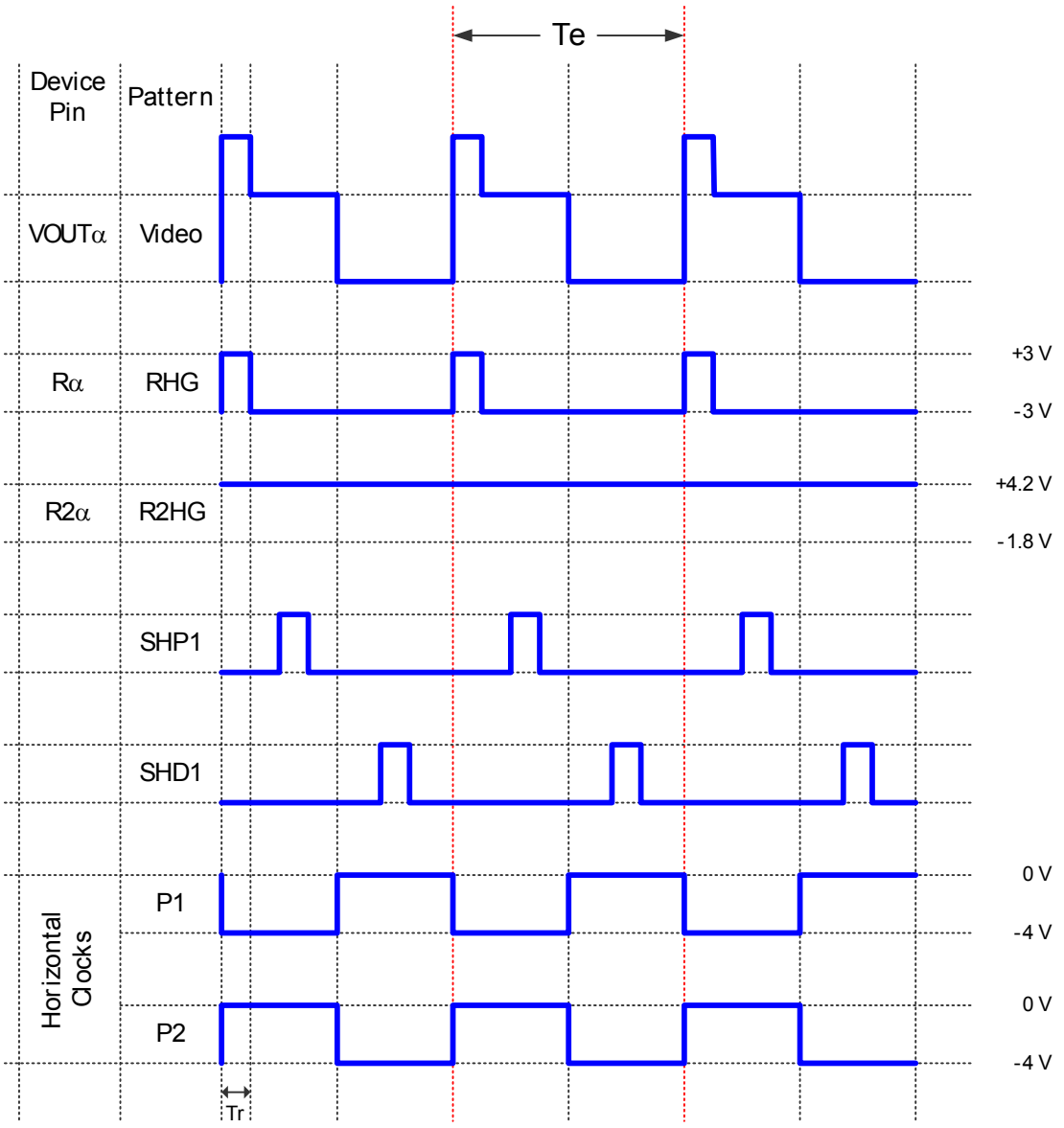


Figure 36: Pixel Timing Diagram – Full Resolution – High Gain

Pixel Timing – Full Resolution – Low Gain Pixel Timing

Use this pixel timing to read out every pixel at low gain. If the sensor is to be permanently operated at low gain, the Ra, Rb, Rc and Rd pins should be set to any DC voltage between +3 and +5V. The SHP1 and SHD1 pulses indicate where the camera electronics should sample the video waveform. The SHP1 and SHD1 pulses are not applied to the image sensor.

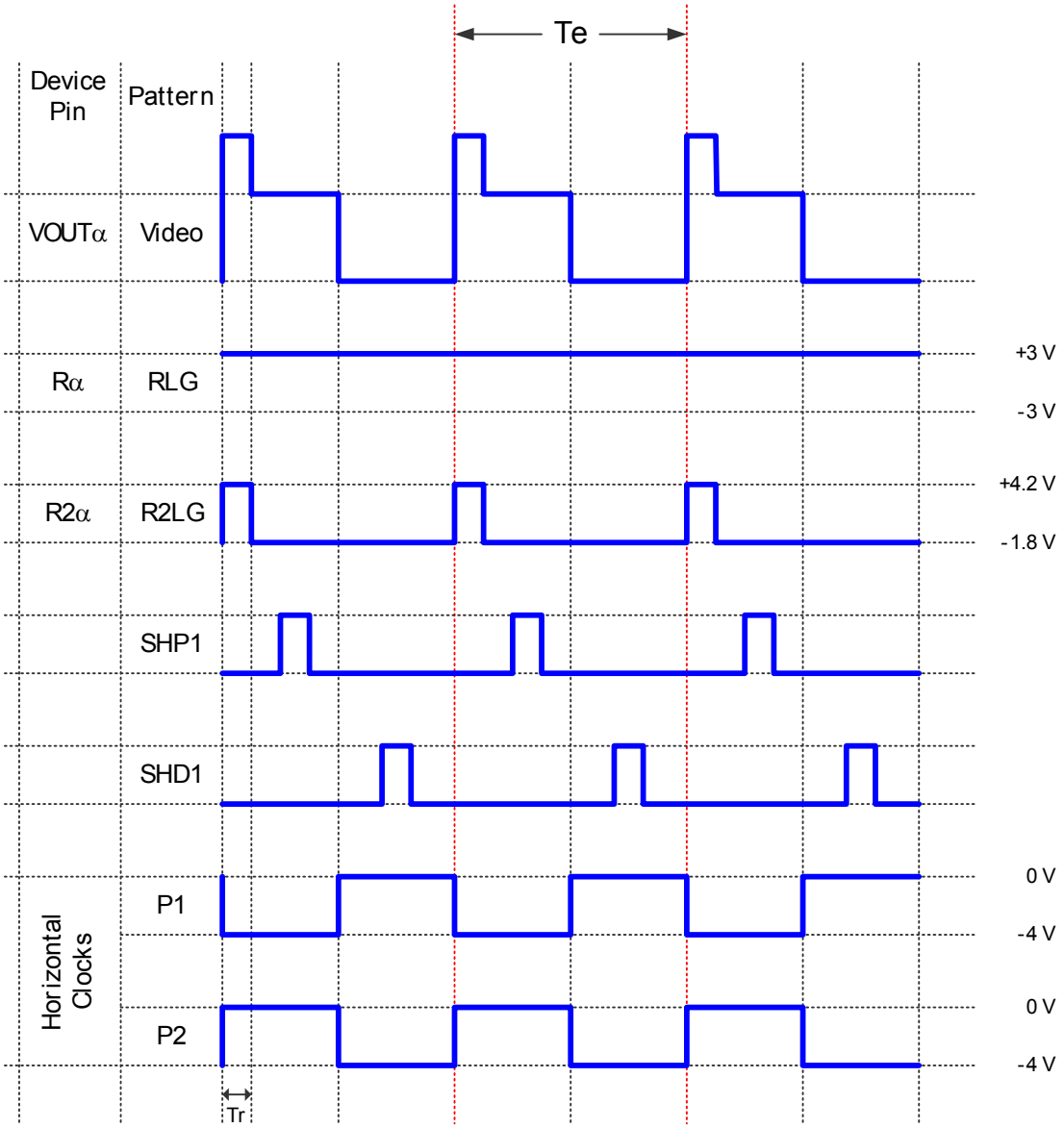


Figure 37: Pixel Timing Diagram – Full Resolution – Low Gain

Pixel Timing – 1/4 Resolution – High Gain Pixel Timing

Use this timing to read out two pixels summed on the output amplifier sense node at high gain. If the sensor is to be permanently operated at high gain, the R2ab and R2cd pins can be left floating or set to any DC voltage between +3V and +5V. Note the R2ab and R2cd pins are internally biased to +4.3V when left floating. The SHPQ and SHDQ pulses indicate where the camera electronics should sample the video waveform. The SHPQ and SHDQ pulses are not applied to the image sensor.

The Ra, Rb, Rc, and Rd pins are pulsed at half the frequency of the horizontal CCD clocks. This causes two pixels to be summed on the output amplifier sense node. The SHPQ and SHDQ clocks are also half the frequency of the horizontal CCD clocks.

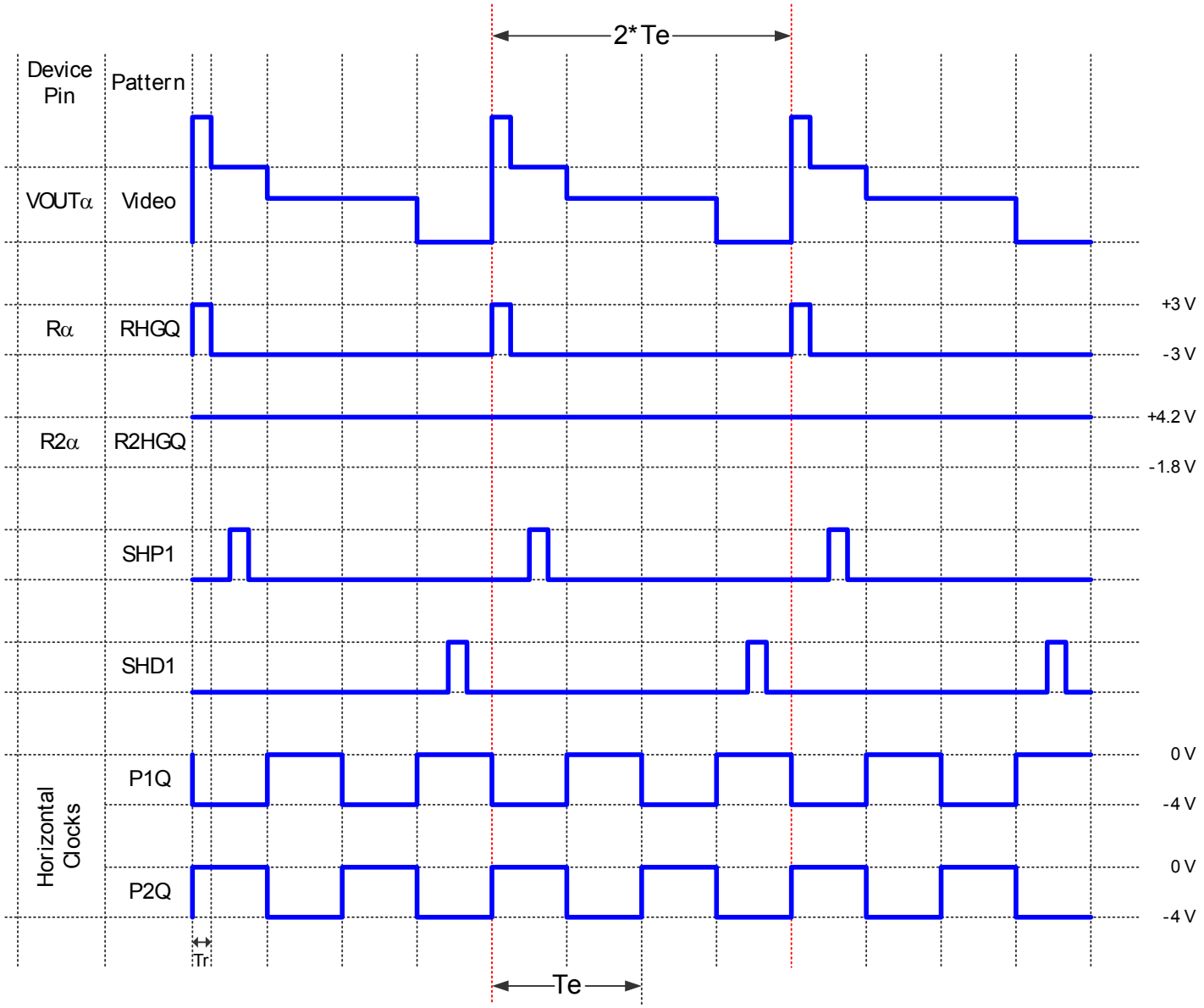


Figure 38: Pixel Timing Diagram – 1/4 Resolution – High Gain

Pixel Timing – 1/4 Resolution – Low Gain Pixel Timing

Use this timing to read out two pixels summed on the output amplifier sense node at low gain. If the sensor is to be permanently operated at low gain, the Ra, Rb, Rc and Rd pins can be set to any DC voltage between +3V and +5V. The SHPQ and SHDQ pulses indicate where the camera electronics should sample the video waveform. The SHPQ and SHDQ pulses are not applied to the image sensor.

The R2ab and R2cd pins are pulsed at half the frequency of the horizontal CCD clocks. This causes two pixels to be summed on the output amplifier sense node. The SHPQ and SHDQ clocks are also half the frequency of the horizontal CCD clocks.

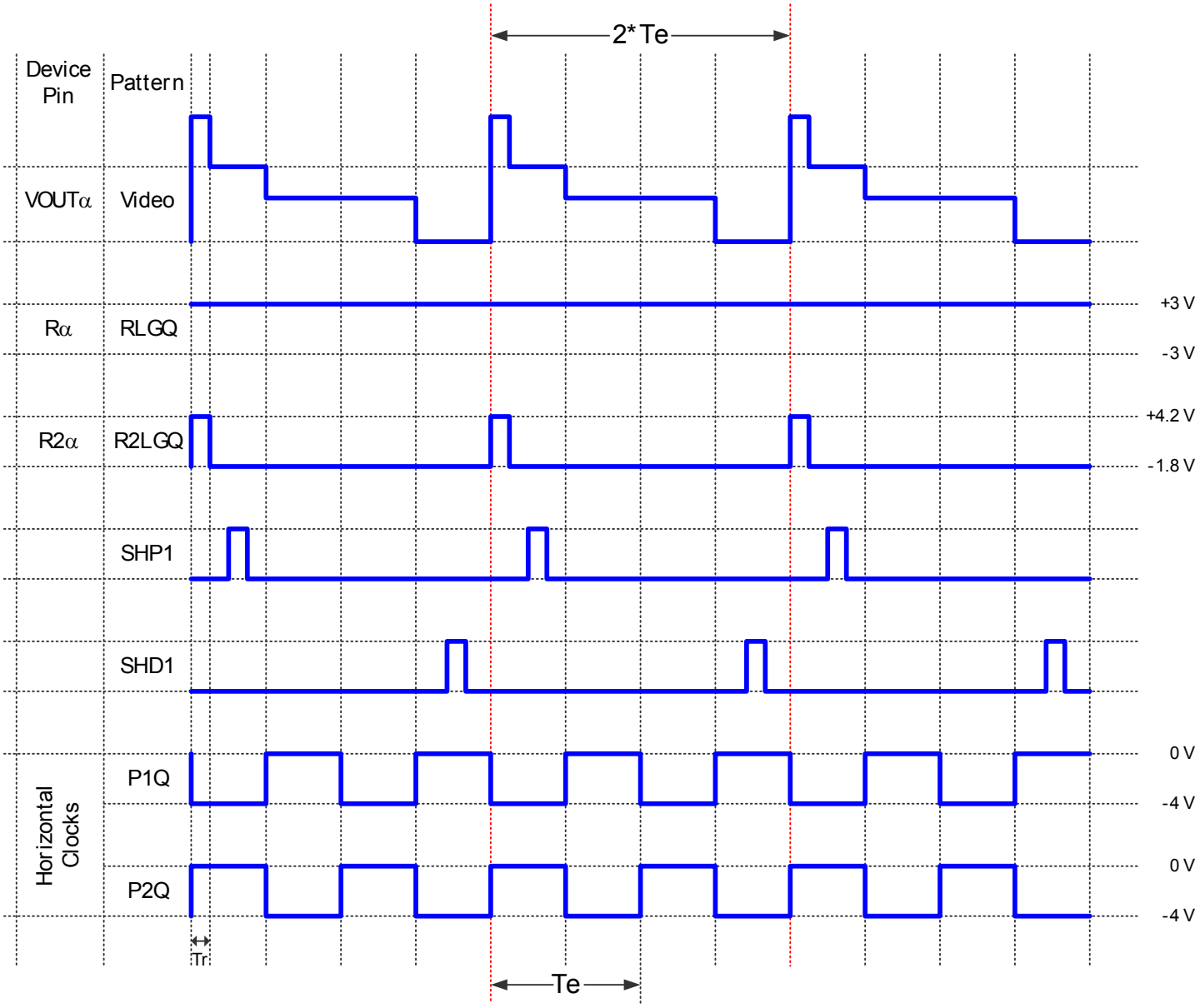


Figure 39: Pixel Timing Diagram – 1/4 Resolution – Low Gain

XLDR Pixel Timing

To operate the sensor in extended linear dynamic range (XLDR) mode, the following pixel timing should be used. This mode requires two sets of analog front end (AFE) signal processing electronic units for each output. As shown in Figure 40 one AFE samples the pixel at low gain (SHPLG and SHDLG) and the other AFE samples the pixel at high gain (SHPHG and SHDHG).

Two HCCD pixels are summed on the output amplifier node to obtain enough charge to fully use the 82 dB range of the XLDR timing. Combined with two-line VCCD summing, a total of 160,000 electrons of signal (4x 40,000) can be sampled with 12 electrons or less noise. Note that a linear dynamic range of 82 dB is very large. Ensure that the camera optics is capable of focusing an 82 dB dynamic range image on the sensor. Lens flare caused by inexpensive optics or even dust on the lens will limit the dynamic range.

The timing shown in Figure 42 shows the HCCD not being clocked at a constant frequency. If the HCCD cannot be clocked at a variable frequency, then the HCCD may be clocked at a constant frequency (Figure 41) at the expense of about 33% slower frame rate.

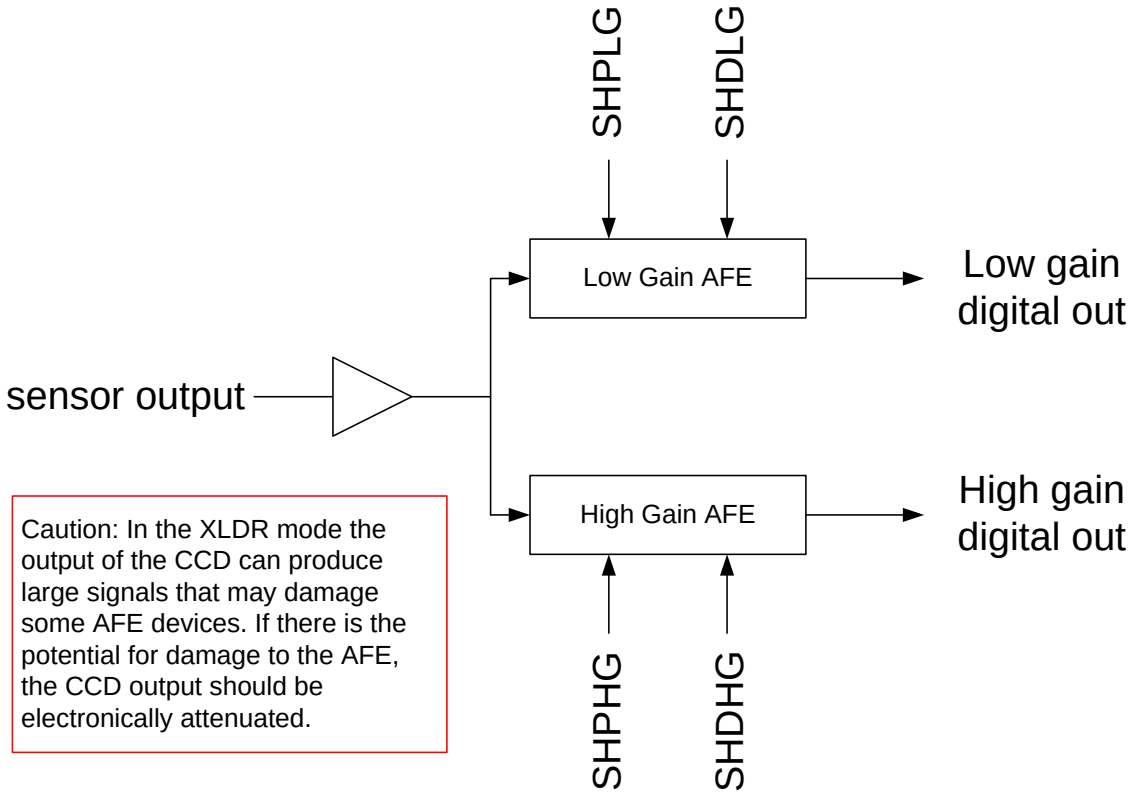


Figure 40: XLDR Timing - AFE Connections Block Diagram

Pixel Timing – 1/4 Resolution – XLDR Pixel Timing – Constant HCCD Timing

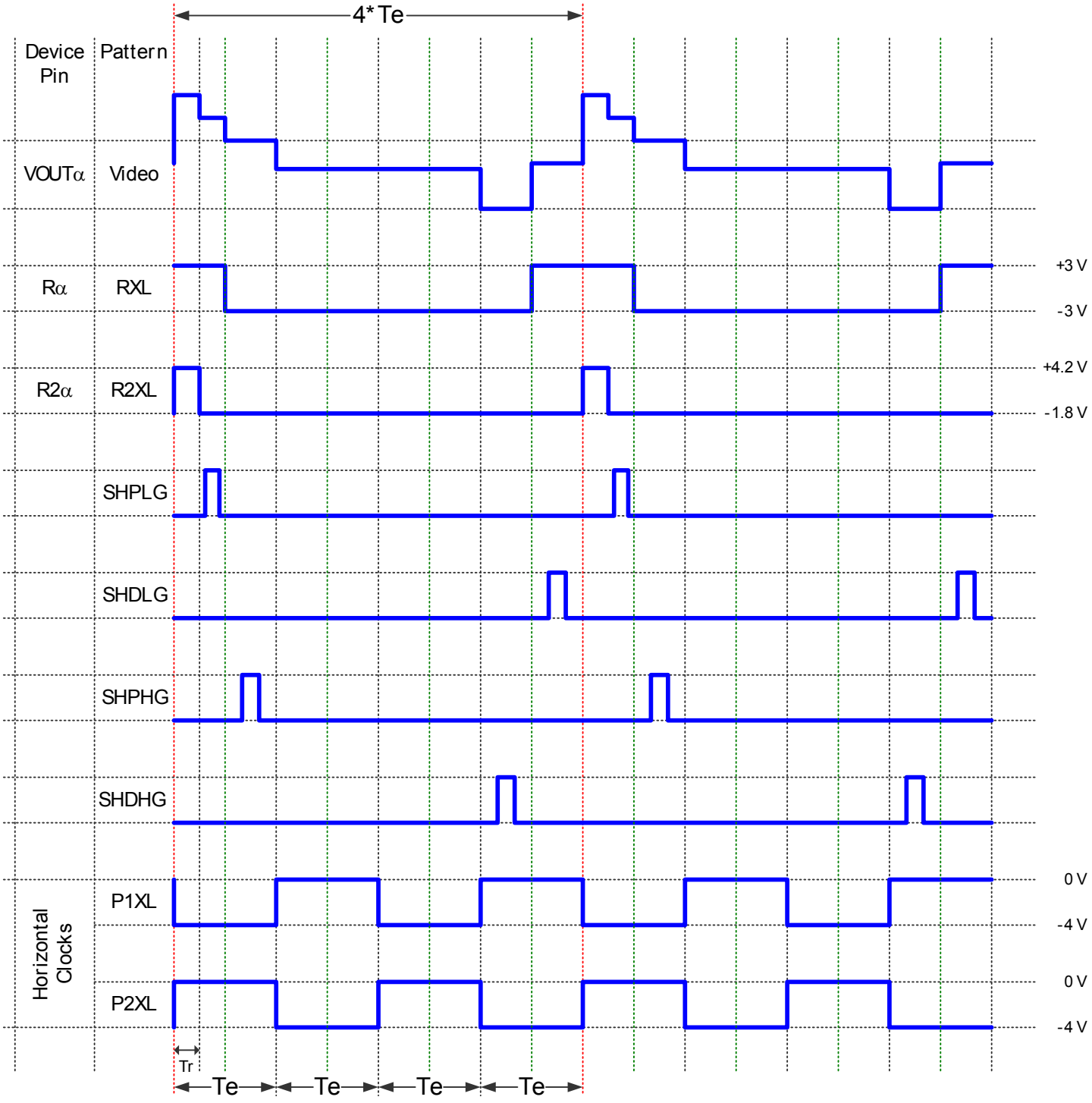


Figure 41: Pixel Timing Diagram – 1/4 Resolution – XLDR – Constant HCCD Timing

Pixel Timing – 1/4 Resolution – XLDR Pixel Timing – Variable HCCD Timing

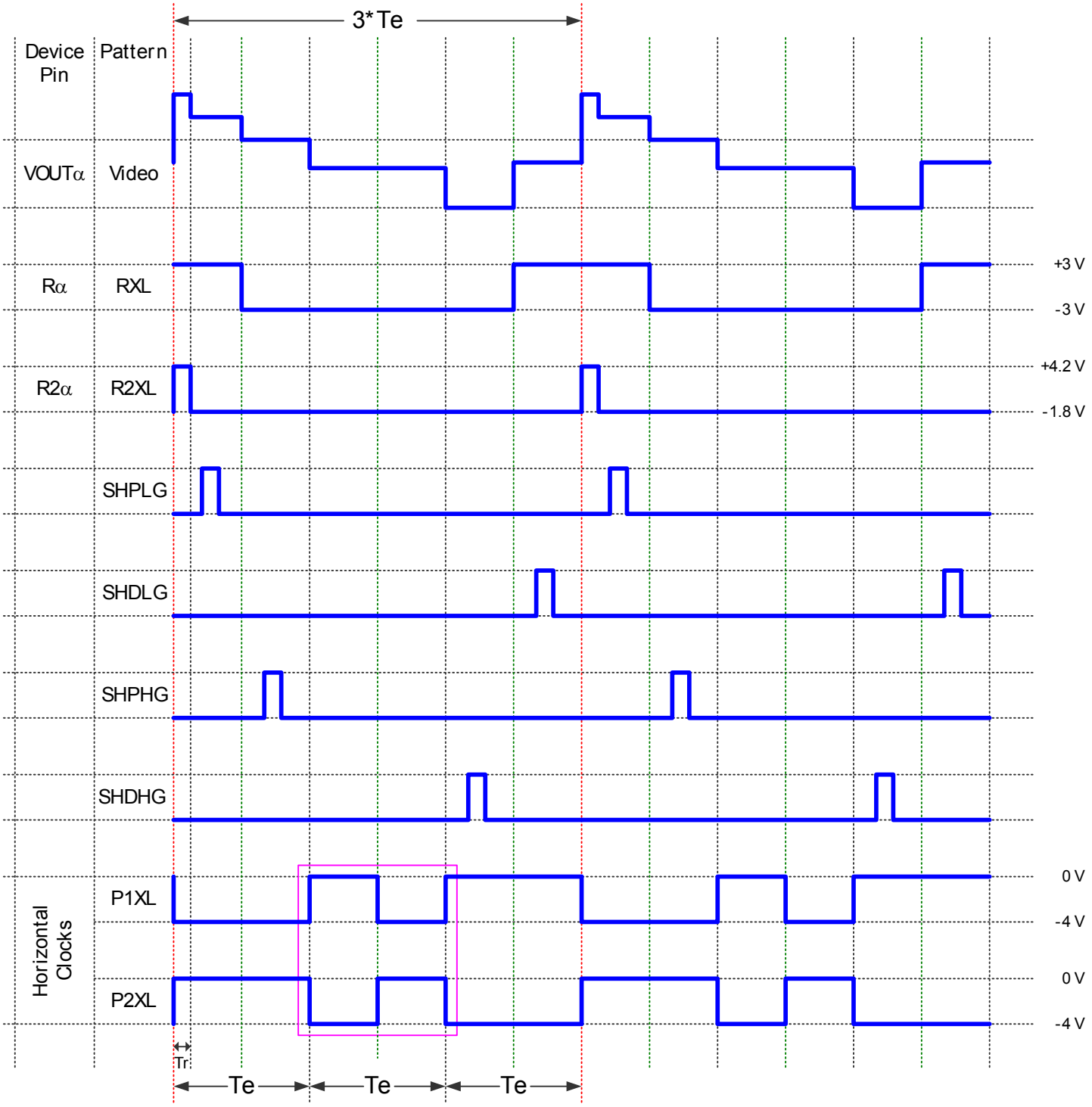


Figure 42: Pixel Timing Diagram – 1/4 Resolution – XLDR – Variable HCCD Timing

VCCD Clock Edge Alignment

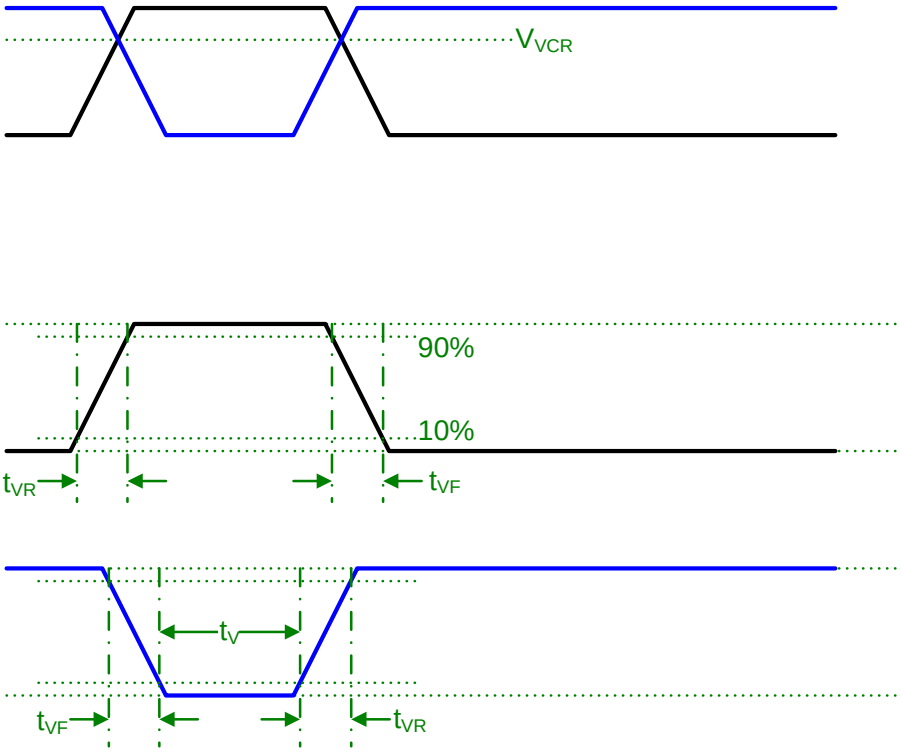


Figure 43: VCCD Clock Rise Time, Fall Time, and Edge Alignment

Storage and Handling

Storage Conditions

Description	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_{ST}	-55	+80	°C	1
Humidity	RH	5	90	%	2

Notes:
1. Long-term storage toward the maximum temperature will accelerate color filter degradation.
2. T=25°C. Excessive humidity will degrade MTTF.

ESD

1. This device contains limited protection against Electrostatic Discharge (ESD). ESD events may cause irreparable damage to a CCD image sensor either immediately or well after the ESD event occurred. Failure to protect the sensor from electrostatic discharge may affect device performance and reliability.
2. Devices should be handled in accordance with strict ESD procedures for Class 0 (<250V per JESD22 Human Body Model test), or Class A (<200V JESD22 Machine Model test) devices. Devices are shipped in static-safe containers and should only be handled at static-safe workstations.
3. See Application Note *Image Sensor Handling Best Practices* for proper handling and grounding procedures. This application note also contains workplace recommendations to minimize electrostatic discharge.
4. Store devices in containers made of electro-conductive materials.

Cover Glass Care and Cleanliness

1. The cover glass is highly susceptible to particles and other contamination. Perform all assembly operations in a clean environment.
2. Touching the cover glass must be avoided.
3. Improper cleaning of the cover glass may damage these devices. Refer to Application Note *Image Sensor Handling Best Practices*.

Environmental Exposure

1. Extremely bright light can potentially harm CCD image sensors. Do not expose to strong sunlight for long periods of time, as the color filters and/or microlenses may become discolored. In addition, long time exposures to a static high contrast scene should be avoided. Localized changes in response may occur from color filter/microlens aging. For Interline devices, refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible lighting Conditions*.
2. Exposure to temperatures exceeding maximum specified levels should be avoided for storage and operation, as device performance and reliability may be affected.
3. Avoid sudden temperature changes.
4. Exposure to excessive humidity may affect device characteristics and may alter device performance and reliability, and therefore should be avoided.
5. Avoid storage of the product in the presence of dust or corrosive agents or gases, as deterioration of lead solderability may occur. It is advised that the solderability of the device leads be assessed after an extended period of storage, over one year.

Soldering Recommendations

1. The soldering iron tip temperature is not to exceed 370 °C. Higher temperatures may alter device performance and reliability.
2. Flow soldering method is not recommended. Solder dipping can cause damage to the glass and harm the imaging capability of the device. Recommended method is by partial heating using a grounded 30W soldering iron. Heat each pin for less than 2 seconds duration.

Mechanical Information

COMPLETED ASSEMBLY

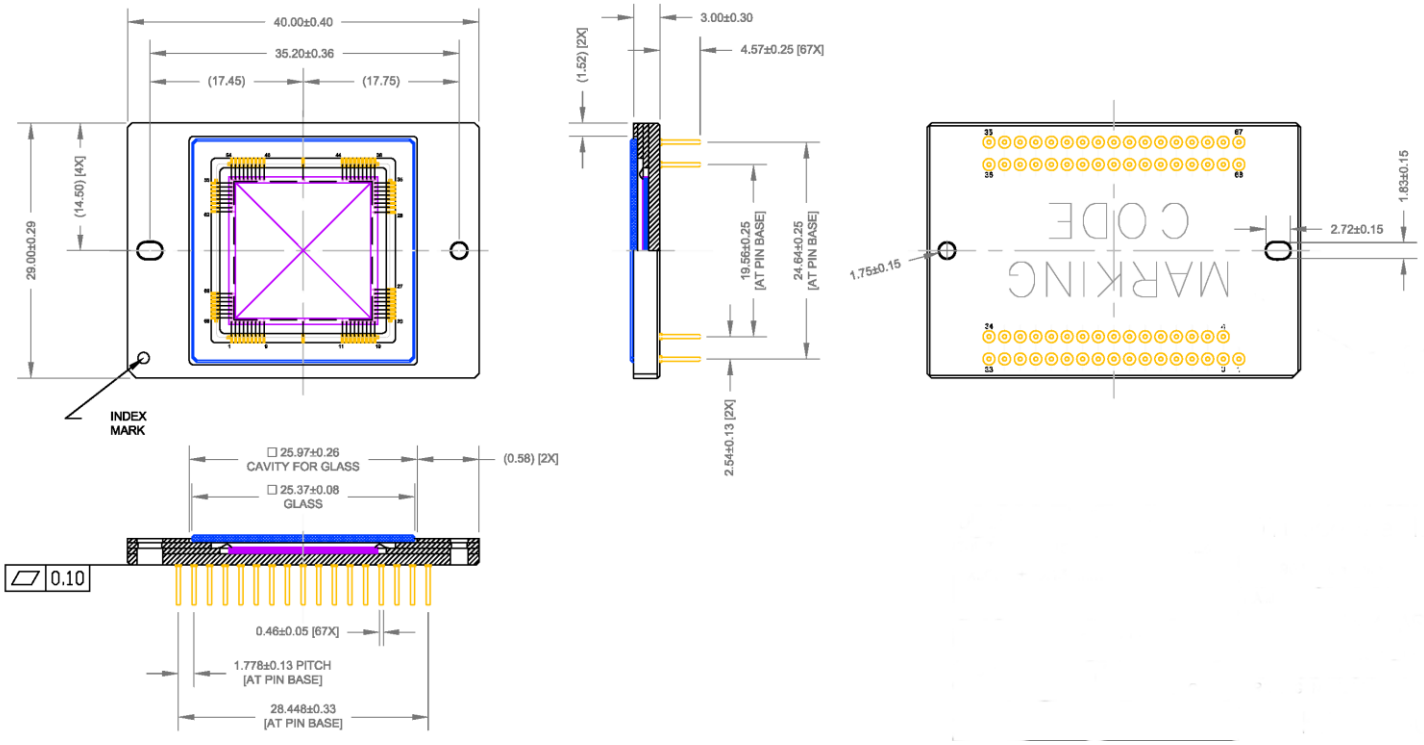


Figure 44: Completed Assembly (1 of 2)

Notes:

1. See Ordering Information for marking code.
2. No materials to interfere with clearance through package holes.
3. Units: mm

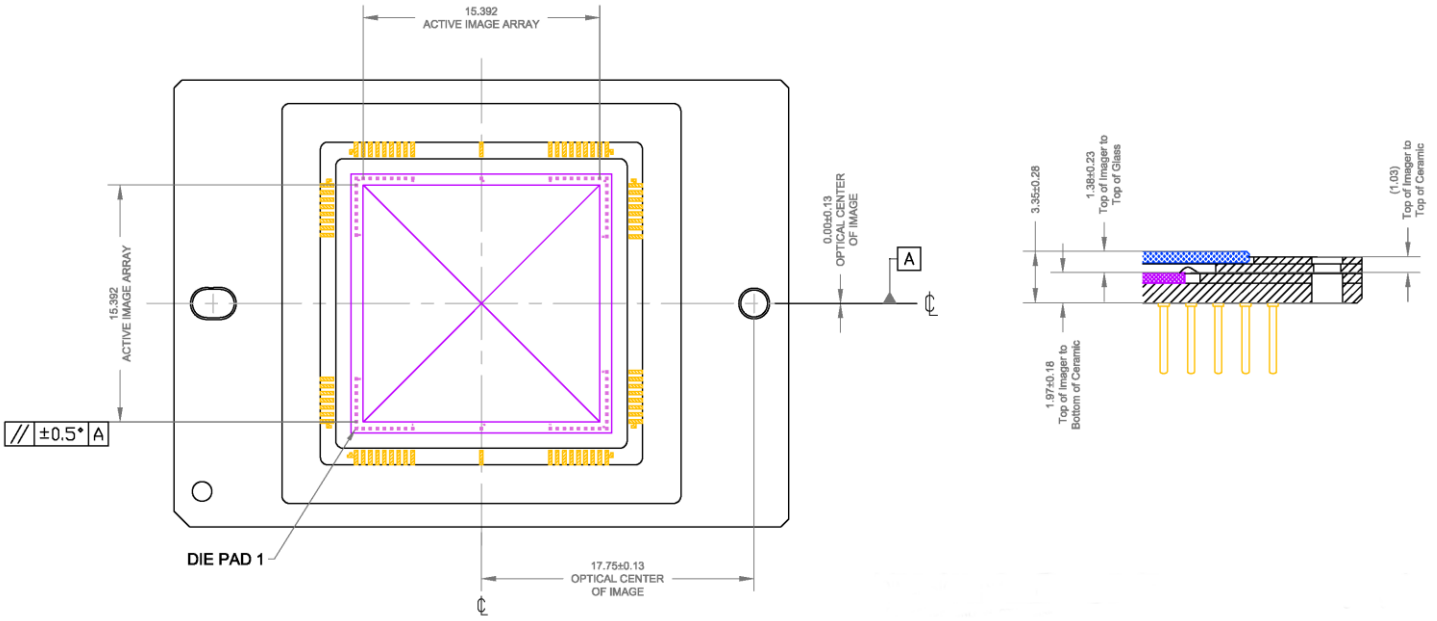


Figure 45: Completed Assembly (2 of 2)

Notes:
1. Optical center of image is nominally at the package center
2. Units: mm

Cover Glass

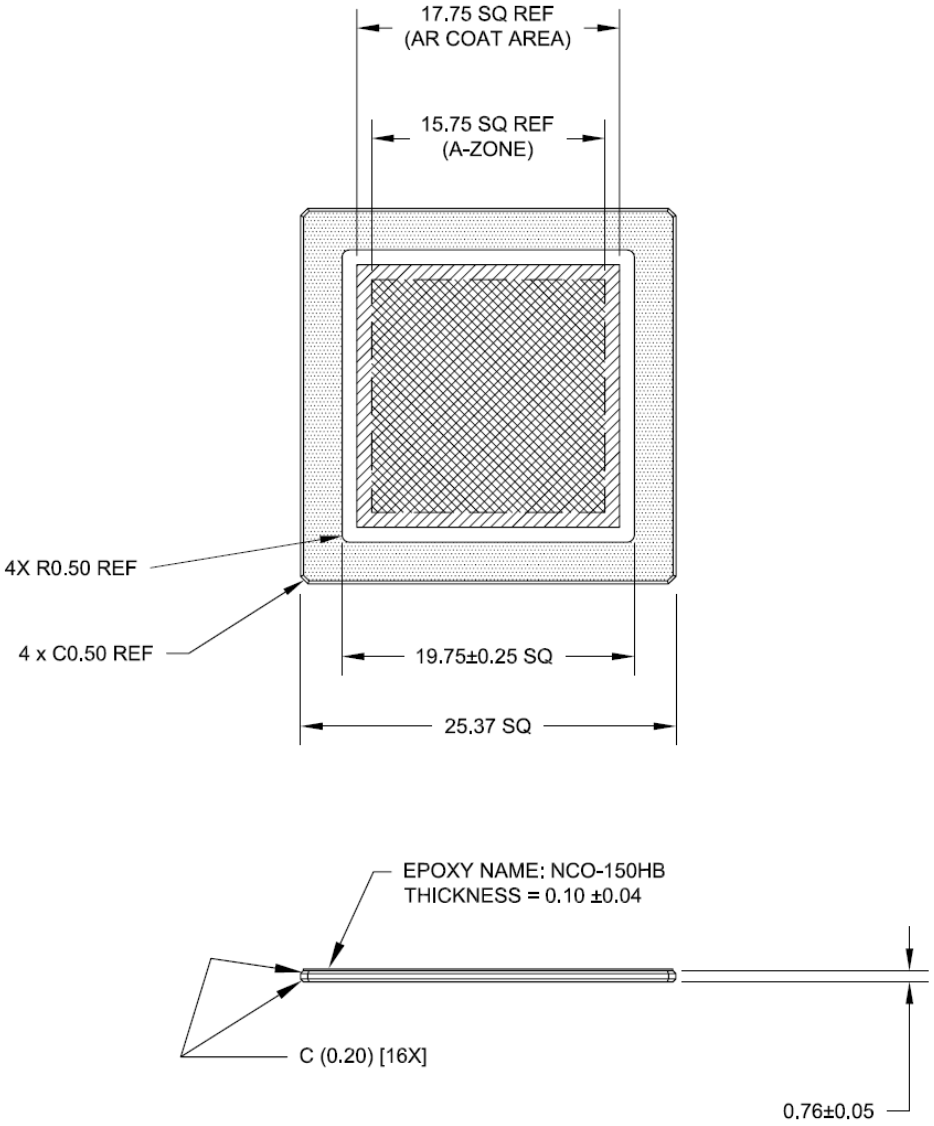


Figure 46: Cover Glass

Notes:

1. Substrate = Schott D263T eco
2. Dust, Scratch, Inclusion Specification:10µm maximum size in Zone A
3. MAR coated both sides
4. Spectral Transmission
    a. T > 98.0% 420-435 nm
    b. T > 99.2% 435-630 nm
    c. T > 98.0% 630-680 nm
5. Units: mm

COVER GLASS TRANSMISSION

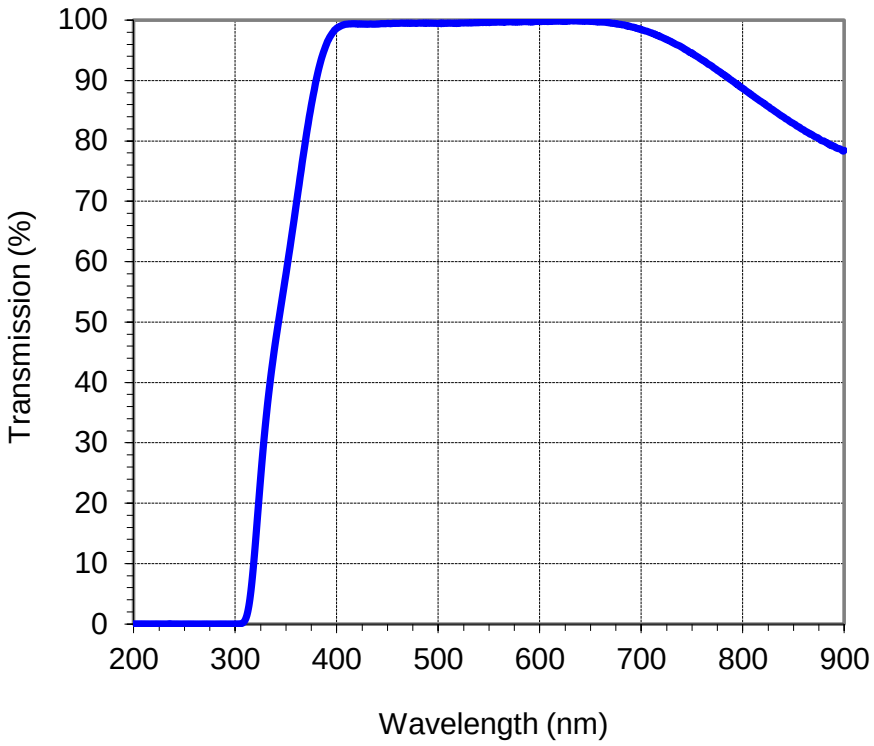


Figure 47: Cover Glass Transmission

Quality Assurance and Reliability

Quality and Reliability

All image sensors conform to the specifications stated in this document. This is accomplished through a combination of statistical process control and visual inspection and electrical testing at key points of the manufacturing process, using industry standard methods. Information concerning the quality assurance and reliability testing procedures and results are available from ON Semiconductor upon request. For further information refer to Application Note *Quality and Reliability*.

Replacement

All devices are warranted against failure in accordance with the *Terms of Sale*. Devices that fail due to mechanical and electrical damage caused by the customer will not be replaced.

Liability of the Supplier

A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer. Product liability is limited to the cost of the defective item, as defined in the *Terms of Sale*.

Liability of the Customer

Damage from mishandling (scratches or breakage), electrostatic discharge (ESD), or other electrical misuse of the device beyond the stated operating or storage limits, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

Test Data Retention

Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

Mechanical

The device assembly drawing is provided as a reference.

ON Semiconductor reserves the right to change any information contained herein without notice. All information furnished by ON Semiconductor is believed to be accurate.

Life Support Applications Policy

ON Semiconductor image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of ON Semiconductor.

Revision Changes

Revision Number	Description of Changes
1.0	• Initial Release
2.0	• Added Monochrome, Telecentric Microlens, PGA Package, Taped Clear Cover Glass with AR coating (both sides) part numbers to the Ordering Information table • Removed Td (VCCD Transfer Delay) from Timing Requirements and Characteristics table • Corrected Vertical CCD clock levels in Pixel Timing table from -9V to -8V
2.1	• Updated branding

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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P.O. Box 5163, Denver, Colorado 80217 USA
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Email: orderlit@onsemi.com

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ON Semiconductor Website: **www.onsemi.com**

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For additional information, please contact your local Sales Representative